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APPLICATION NOTE

AP-17

Application of the Intel® 2708 8K Erasable PROM

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Contents

INTRODUCTION

The Intel® 2708 is a static 8192-bit (1024 X 8) Erasable Programmable Read Only Memory, or EPROM. The device is packaged in a standard 24-pin package, which has a transparent lid to allow erasure in a manner similar to the Intel® 1702A. Maximum access time is 450 ns. The device requires three power supplies, ±5V and +12V, for normal read cycles; while for programming a 26V pulse is required on the Program pin.

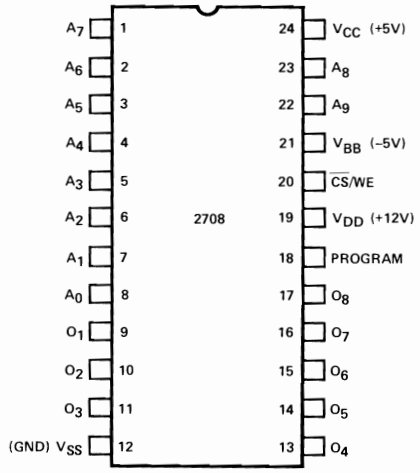
The address inputs and data I/Os are TTL compatible during read and programming. The data outputs are three state to facilitate memory expansion by OR-tying. Initially, and after each erasure, the device contains all "1's". Programming, or introducing "0's", is accomplished by: applying TTL level addresses and TTL level data; a +12V Write Enable signal; then sequencing through all addresses consecutively a minimum of 100 times, applying a 26V program pulse at each address. ALL ADDRESSES MUST BE PROGRAMMED DURING EACH PROGRAMMING SESSION; PROGRAMMING OF SINGLE WORDS OR SMALL BLOCKS OF WORDS IS NOT ALLOWED. As discussed in detail in the PROGRAMMING section, approximately 100 seconds are required to program the entire device.

DEVICE DESCRIPTION

The device is packaged in an industry standard 24-pin package as shown in Figure 1. The Program pin (18) receives 26V pulses during programming; during read operations it must be connected to V_{SS} (GND) or held at V_{IL}.

Pin 20, the $\overline{CS}$/WE connection, serves three functions. When at V_{IL} (0V) the device is selected for normal read operation; when at V_{IH} (3.0V min) the device is deselected and the outputs are placed in the high impedance state; and when at V_{IHW} (11.4V min) the device is Write Enabled and ready to receive program pulses.

A block diagram of the 2708 is shown in Figure 2. The low order address bits (A_0–A_3) perform column (or Y) selection, while the high order address



PIN NAMES

A_1-A_9	ADDRESS INPUTS
O_1-O_8	DATA OUTPUTS
CS/WE	CHIP SELECT/WRITE ENABLE INPUT

Figure 1. 2708 Pin Configuration

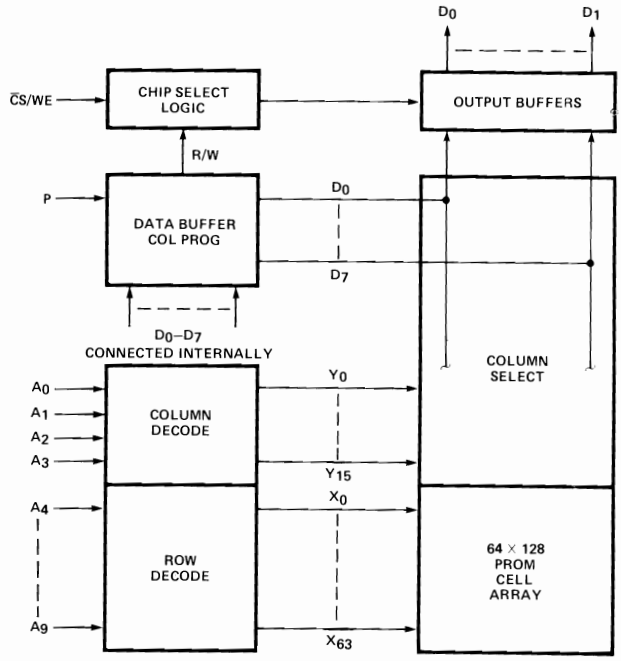


Figure 2. Detailed Block Diagram

Table I. 2708 Pin Connections and Functions

Function / Pin Number / Mode	Data I/O 9–11, 13–17	Address Inputs 1–7, 23, 22	V_{SS} (GND) 12	Program 18	V_{DD} Supply 19	$\overline{CS}$/WE 20	V_{BB} Supply 21	V_{CC} Supply 24
Read	D_{OUT}	A_{IN}	GND	GND	+12V	V_{IL}	-5V	+5V
Deselect	High Impedance	Don't Care	GND	GND	+12V	V_{IH}	-5V	+5V
Program	D_{IN}	A_{IN}	GND	Pulsed +26V	+12V	V_{IHW}	-5V	+5V

bits (A_4–A_9) perform the row (or X) selection. Table I assists in determining the proper voltage connections for the three modes of operation; Read, Deselect and Program.

Cell Description

The heart of the 2708 is the single transistor stacked gate cell, implemented with two layer polysilicon. The cell consists of a bottom floating gate and a top select gate, as shown in Figure 3. The top gate is connected to the row decoder, while the floating gate is used for charge storage. The cell is programmed by injection of high energy electrons through the oxide and onto the floating gate. Once there the charge is trapped, as there are no electrical connections to this floating gate. The presence of charge on the floating gate causes a shift to the cell threshold, as shown in Figure 4. In the initial state the cell has a very low threshold and selection of the cell, by way of the top select gate, will cause the transistor to turn on. Programming shifts the threshold to a higher level and selection of the cell will not allow it to turn on. The status of the cell is determined by examining its state at the sense threshold, also indicated in Figure 4. If a "1" is programmed into the cell, selection will allow a higher current to flow between the source and drain than if a "0" is programmed into the cell.

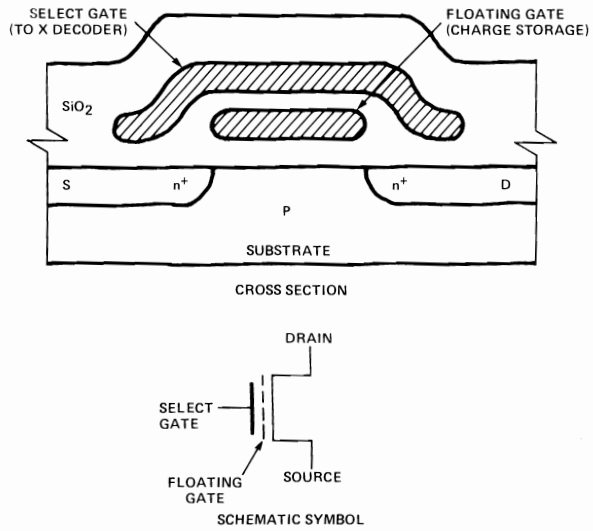


Figure 3. 2708 Storage Cell

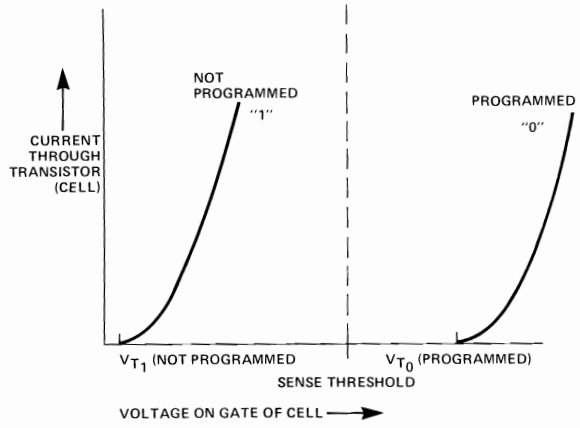


Figure 4. Storage Cell Threshold Shift

As there are no electrical connections to the floating gate, erasure must be accomplished by non-electrical means. Illumination of the cell with ultraviolet light of the correct frequency (2537Å) and duration will impart sufficient photon energy to the trapped electrons to allow them to overcome the inherent energy barrier and be transported through the oxide to the substrate.

Memory Array Operation

The cells described in the previous paragraph are interconnected to form a 64 X 128 matrix, or array, as shown in Figure 5. Access to a particular cell is described as follows: When the Row Address is stable, one row is selected, turning on the row line to all 128 cells in the row. The Column Address connects 8 of the 64 column lines to their respective sense amplifiers. The row line provides bias to all the top gates in a particular selected row, and, depending on the state of the cells, the column lines will be left at the precharged level (for a programmed "0") or will be discharged, pulling the column lines down to a low level (for a programmed "1"). To provide the very fast Chip Select to Output Delay time (t_{CO}) of 120 ns, all of the sense amplifiers are turned on when the device is deselected, and, when $\overline{CS}/WE$ reaches V_{IL}, those which are not selected are turned off, and the remaining eight amplifiers convert the charge on the column lines to TTL output levels by way of the output buffers.

During programming the selected row and column lines are pulsed to approximately 26 volts and the floating gate is charged as was described in the previous section. It is the presence of these 26V pulses on the interconnected top gates that lead to the requirement that ALL ADDRESSES MUST BE PROGRAMMED SEQUENTIALLY; PROGRAMMING OF SINGLE WORDS OR SMALL BLOCKS OF WORDS IS NOT ALLOWED, as transients may be generated that could partially alter the charge state of the cell.

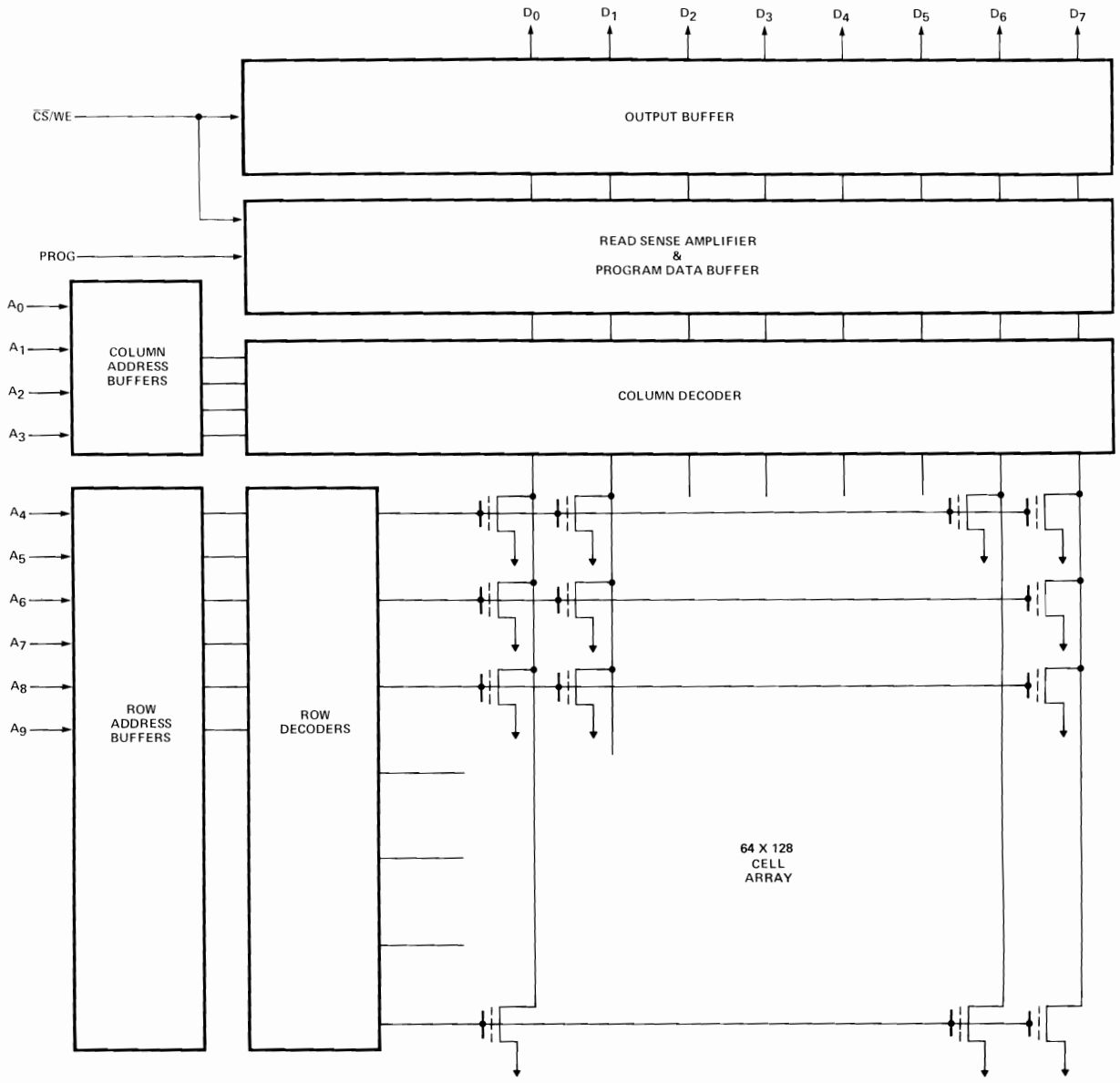


Figure 5. Expanded Block Diagram

Output Buffer

The equivalent schematic of the Output Buffer is shown in Figure 6. As is shown, the output buffer consists of a pair of MOS transistors, connected in a push-pull configuration. $\overline{CS}$ enables both transistors when true, while when $\overline{CS}$ is false both output devices are turned off, providing three state output operation. The output buffer will provide a V_{OL} of 0.45V at an I_{OL} of 1.6 mA, and a V_{OH} of 2.4V at −1.0 mA.

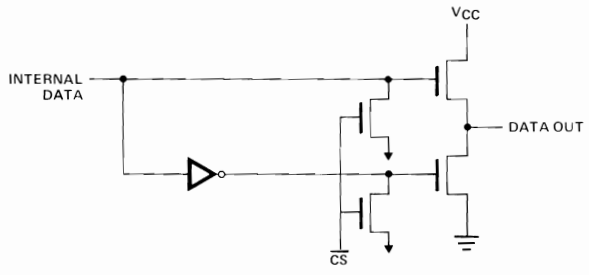


Figure 6. 2708 Output Buffer

Table II. D.C. Read Mode Characteristics

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions
I_{LI}	Address and Chip Select Input Sink Current		1	10	μA	V_{IN} = 5.25 V or V_{IN} = V_{IL}
I_{LO}	Output Leakage Current		1	10	μA	V_{OUT} = 5.25V, $\overline{CS}$/WE = 5V
I_{DD}[2]	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents:
I_{CC}[2]	V_{CC} Supply Current		6	10	mA	All Inputs High
I_{BB}[2]	V_{BB} Supply Current		30	45	mA	$\overline{CS}$/WE = 5V; T_A = 0°C
V_{IL}	Input Low Voltage	V_{SS}		0.65	V	
V_{IH}	Input High Voltage	3.0		V_{CC}+1	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH1}	Output High Voltage	3.7			V	I_{OH} = -100μA
V_{OH2}	Output High Voltage	2.4			V	I_{OH} = -1mA
P_D	Power Dissipation			800	mW	T_A = 70°C

NOTES: 1. Typical values are for T_A = 25°C and nominal supply voltages.
2. The total power dissipation of the 2708 is specified at 800 mW. It is not calculable by summing the various currents (I_{DD}, I_{CC}, and I_{BB}) multiplied by their respective voltages since current paths exist between the various power supplies and V_{SS}. The I_{DD}, I_{CC}, and I_{BB} currents should be used to determine power supply capacity only.

D.C. DEVICE CHARACTERISTICS

Only those D.C. Characteristics that require special attention by the user are presented in this section. The reader is referred to the 2708 device data sheet for further details. The pertinent D.C. device specifications are tabulated in Table II.

The 2708 requires three power supplies, +12V and ±5V. The device is rated to meet all applicable specifications with these supplies held within ±5% of their normal value. The Absolute Maximum Ratings in the data sheet are the maximum that the various device parameters can withstand and should not be exceeded during any phase of device operation, including programming.

Read Mode

The range of values of currents from the three power supplies, V_{DD} (+12V), V_{CC} (+5V) and V_{BB} (−5V) are shown in Table II, presented for the worst case conditions; i.e., $\overline{CS}$/WE = 5V and T_A = 0°C. The I_{DD}, I_{CC} and I_{BB} data presented indicates the maximum current drawn by the respective power input. These inputs cannot simultaneously draw maximum current. Refer to the APPLICATIONS SECTION for measured laboratory data of the interactive effects of switching the various supplies off to conserve power.

The addresses are TTL compatible, requiring V_{IL} between V_{SS} and 0.65V and V_{IH} between 3V and V_{CC} + 1. Care should be exercised in selecting address buffers to insure the minimum V_{IH} level is met by use of appropriate TTL circuit elements or pull-up resistors to V_{CC}.

During the Read mode, the $\overline{CS}$/WE input (pin 20) is also TTL compatible; however, the V_{IL} and V_{IH} requirements for the address inputs are still applicable.

The outputs are also TTL compatible, producing a V_{OL} of 0.45V maximum @ 1.6 mA and a V_{OH} of 3.7V with −100 μA capability, or 2.4V with −1 mA capability. Typical output sink current is plotted in Figure 7 as a function of the output voltage and temperature for applications requiring higher than normal I_{OL} currents.

Figure 8 illustrates several points regarding the 2708 power supply currents. First of all, as with all MOS devices, the power supply currents will decrease as a function of increasing temperature. The second point is that the current requirements of the device increase when it is deselected, i.e., when $\overline{CS}$/WE is at V_{IH}. The reason for this is that in order to meet the very fast t_{CO} time of 120 ns, all of the decoders and output stages are turned on when $\overline{CS}$/WE is at V_{IH}, and the decoders deselect those that are not required for the given data cycle. The graph also illustrates that the V_{DD} power supply is the most logical supply to be selected for switching to reduce power. Of course, if the system configuration permits, $\overline{CS}$/WE can be tied to V_{SS} to reduce power.

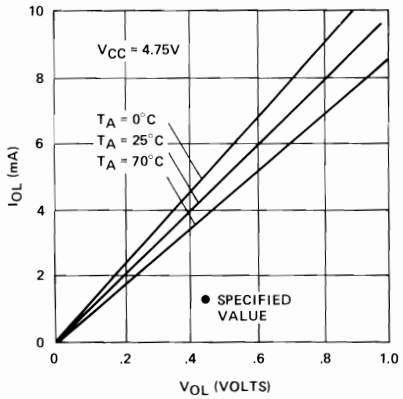


Figure 7. 2708 Typical Output Sink Current vs. Output Voltage

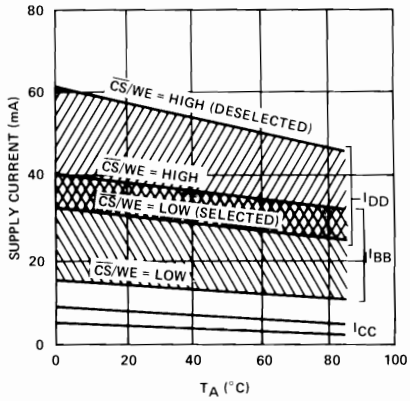


Figure 8. 2708 Power Supply Currents

Table III. D.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_{LI}	Address and $\overline{CS}$/WE Input Sink Current			10	μA	V_{IN} = 5.25V
I_{IPL}	Program Pulse Source Current			3	mA	
I_{IPH}	Program Pulse Sink Current			20	mA	
I_{DD}	V_{DD} Supply Current		50	65	mA	Worst Case Supply Currents:
I_{CC}	V_{CC} Supply Current		6	10	mA	All Inputs High
I_{BB}	V_{BB} Supply Current		30	45	mA	$\overline{CS}$/WE = 5V; T_A = 0°C
V_{IL}	Input Low Level (except Program)	V_{SS}		0.65	V	
V_{IH}	Input High Level for all Addresses and Data	3.0		V_{CC}+1	V	
V_{IHW}	$\overline{CS}$/WE Input High Level	11.4		12.6	V	Referenced to V_{SS}
V_{IHP}	Program Pulse High Level	25		27	V	Referenced to V_{SS}
V_{ILP}	Program Pulse Low Level	V_{SS}		1	V	V_{IHP} - V_{ILP} = 25V min.

Program Mode

The address and data inputs are low level compatible during programming, with the same requirements of V_{IL} and V_{IH} as for the Read mode. The D.C. characteristics for programming are shown in Table III. To enable the device for programming, the $\overline{CS}$/WE pin is raised to V_{IHW}, (11.4V). If the system requirements dictate that the device stay in the same socket or location for both reading and programming, it should be recalled that this pin will require three input levels: V_{IL} of V_{SS} to 0.65V to select the device for a read operation, a V_{IH} of 3V to V_{CC} +1 to deselct the device and place the output in the high impedance state, and a V_{IHW} of 11.4 to 12.6V to Write Enable, or allow programming of the device. Several circuits for generating these three active levels (V_{IL}, V_{IH} and V_{IHW})are shown in the PROGRAMMING section (page 7).

During program operation, the outputs become the data inputs and should be treated as a three state bus. The same V_{IL} and V_{IH} levels apply to the data I/O pins as apply to the address pins.

The program pulse, which is applied to pin 18 during programming, must meet a V_{ILP} requirement (V_{SS} to 1V) and a V_{IHP} requirement (26V ± 1V).

The program pulse source must be capable of supplying a maximum of 20 mA per device when high (V_{IHP}), and be able to withstand the Program Pulse Sink current of 3 mA (I_{IPL}). This sink current should be considered when designing the program pulse driver, as, if a resistive pull-down is used, the voltage drop across the resistor can violate the V_{ILP} max requirement of 1V. It also should be noted that the program pulse will not meet specification if V_{IHP} is taken at its minimum value (25V) and V_{ILP} is taken at its maximum value (1V), as $V_{IHP}-V_{ILP}$ must equal 25 volts minimum. Several circuits are presented in the PROGRAMMING section to provide program pulses which easily meet the 25V minimum requirement for $V_{IHP}-V_{ILP}$.

A.C. DEVICE CHARACTERISTICS

Read Mode

Figure 9, the Read mode timing, indicates the maximum or minimum timing for the various timing parameters. Particular attention should be paid to t_{DF}, chip deselect to output float time. This indicates that the output buffers of the 2708 are not guaranteed to reach the high impedance state until 120 ns after $\overline{CS}$/WE reaches the 2.8V point. If another device attempts to take control of the output node during this time, very high I_{CC} current will be drawn, generating noise on the supply lines and possibly reducing the V_{CC} level such that other devices may become inoperative. t_{DF} is also a factor to consider when switched V_{DD} is used. See the APPLICATIONS section for further discussion.

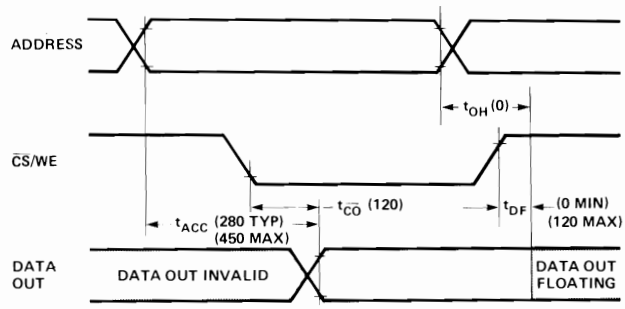


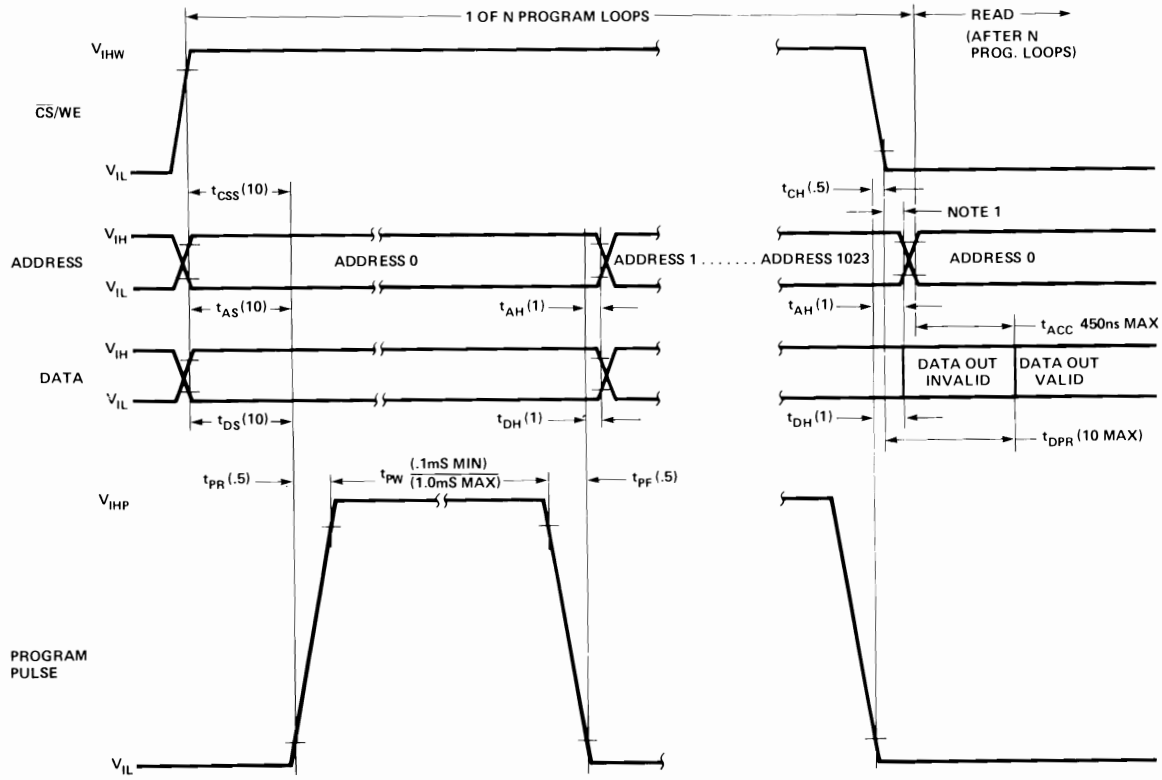
Figure 9. 2708 Read Cycle Waveforms

Program Mode

Figure 10 indicates the Program mode timing, while Table IV tabulates the various programming A.C. parameters.

Several options are available to the user when programming the 2708, as shown in the data sheet. The waveforms shown in Figure 10 represent the most efficient method. The various parameters are self-explanatory; two will be discussed here. The program pulse rise and fall times, t_{PR} and t_{PF}, must be held within the range of 0.5 and 2 μs to minimize the transient coupling effects discussed in the memory array section. This usually requires a series RC network on the output of the program pulse driver to slow down the rise time. Exotic waveform generators are not required. Refer to the PROGRAMMING section for circuit recommendations.

The other parameter of concern to the user is the transition from Program mode to Read mode. If the $\overline{CS}$/WE transition does not occur after the final program pulse transition and before the address transition, as shown in Figure 10, nodes internal to the device will not discharge, causing the output buffers to indicate false data for several milliseconds.



NOTE 1. THE $\overline{CS}$/WE TRANSITION MUST OCCUR AFTER THE PROGRAM PULSE TRANSITION AND BEFORE THE ADDRESS TRANSITION.

NOTE 2. NUMBERS IN ( ) INDICATE MINIMUM TIMING IN μS UNLESS OTHERWISE SPECIFIED.

Figure 10. 2708 Programming Waveforms

Table IV. A.C. Programming Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{AS}	Address Setup Time	10			μs
t_{CSS}	$\overline{CS}$/WE Setup Time	10			μs
t_{DS}	Data Setup Time	10			μs
t_{AH}	Address Hold Time	1			μs
t_{CH}	$\overline{CS}$/WE Hold Time	.5			μs
t_{DH}	Data Hold Time	1			μs
t_{DF}	Chip Deselect to Output Float Delay	0		120	ns
t_{DPR}	Program To Read Delay			10	μs
t_{PW}	Program Pulse Width	.1		1.0	ms
t_{PR}	Program Pulse Rise Time	.5		2.0	μs
t_{PF}	Program Pulse Fall Time	.5		2.0	μs

NOTE: Intel's standard product warranty applies only to devices programmed to specifications described herein.

This will appear as an excessively long t_{DPR}, Program to Read Delay. If the $\overline{CS}$/WE timing is difficult to adjust, providing the binary complement of the first address to be verified before actually verifying will also discharge the internal nodes.

PROGRAMMING

A number of programmers are commercially available that will properly program the 2708. Intel maintains a service whereby commercial programmer manufacturers obtain design approval prior to marketing their device, in order to assure compatibility with Intel specifications. This approval should be verified with the particular programmer manufacturer prior to purchase.

It is also possible to build a programmer as part of the user's system, by adhering to the following description: The device is set up for programming operation by raising the $\overline{CS}$/WE input (pin 20) to V_{IHW} (+12V). The word address is then selected in the same manner as in the Read mode. Data to be programmed are presented, 8 bits in parallel, to the data output pins (O_1–O_8). Logic levels for address and data lines and the supply voltages are the same as for the Read mode. After address and data set up times (t_{AS} and t_{DS}, Fig. 10), one program pulse of width t_{PW} is applied to the program pin (pin 18). This sequence is then repeated for the next address. One pass through all 1024 addresses is defined as a program loop. The number of program loops (N) required is a function of the program pulse width (t_{PW}) according to the formula:

$$N \times t_{PW} \geqslant 100 \text{ ms}$$

where

N is the number of program loops

t_{PW} is the program pulse width.

The width of the program pulse can vary from 0.1 to 1.0 ms. The number of loops (N) can vary from a minimum of 100 (t_{PW} = 1.0 ms) to greater than 1000 (t_{PW} = 0.1 ms), depending on the value chosen for t_{PW}. IT IS NOT PERMITTED TO APPLY N PROGRAM PULSES TO AN ADDRESS AND THEN CHANGE TO THE NEXT ADDRESS AND APPLY N PROGRAM PULSES. THERE MUST BE N SUCCESSIVE LOOPS THROUGH ALL 1024 ADDRESSES.

Referring to the timing diagram, Figure 10, optimum or most efficient programming is achieved when:

$$t_{CSS} = t_{AS} = t_{DS} = 10\ \mu s$$
$$t_{PW} = 1.0 \text{ ms}$$
$$t_{AH} = t_{DH} = 1.0\ \mu s$$
$$t_{PR} = t_{PF} = 0.5\ \mu s$$

and the time for 1 address becomes:

$$t_{AS} + t_{PR} + t_{PW} + t_{PF} + t_{AH} = 1.012 \text{ ms}$$

or, for 100 loops and 1024 addresses, the total time to program an entire device will be 1.012 ms/address × 100 loops × 1024 addresses, or 103.6 sec. Note that the program pulse duty cycle is approximately 99%. Whatever the length of the program pulse, the requirement for making successive passes through all addresses cannot be eliminated.

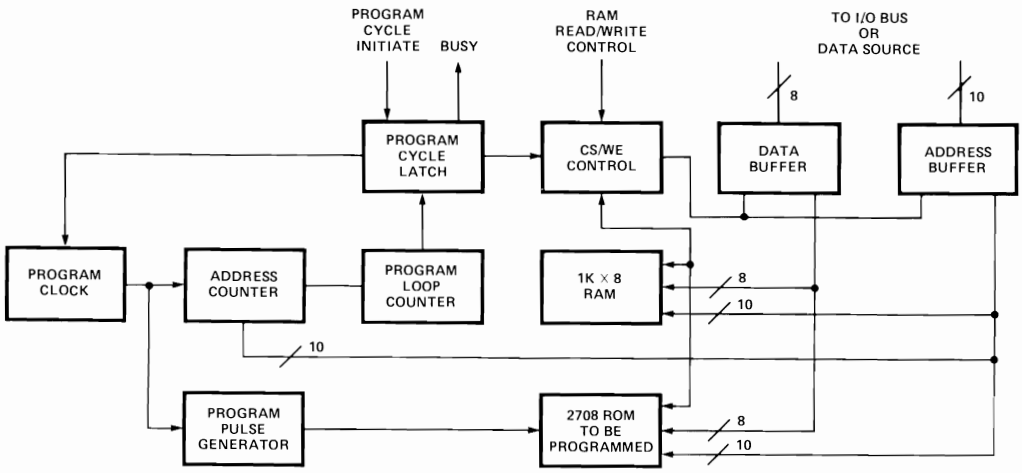


Figure 11. Typical Programming Block Diagram

Typical Programmer

Figure 11 illustrates a block diagram of a typical programmer that meets all the requirements for programming the 2708, as well as facilitating interface to a microcomputer I/O bus if it is desired to use the microprocessor system as a data source. Keyboard entry is also possible, although it does become tedious to manually enter data for 1024 PROM locations.

Operation of the programmer is as follows: While the data is being generated, the RAM Read/Write Control line allows information to pass through the Data Buffer and Address Buffer as in normal microcomputer memory operation. When the data is finalized in the 1K by 8 RAM, a Program Cycle Initiate command is generated, which responds, via the Program Cycle Latch, by generating a Busy signal back to the processor, and disenables the Data and Address Buffers, inhibiting further communication with the I/O bus until the program cycle is complete. The Program Cycle Latch also starts the Program Clock, enables the RAM, and Write Enables the PROM. It also initializes the Address and Program Loop Counters. The Program Clock activates the Program Pulse Generator, causing the information from RAM address A_0 to be programmed into the PROM. The next clock pulse increments the address counter and when the RAM data corresponding to that address is presented to the PROM inputs (outputs during read), it again increments the address counter and continues until the Address Counter overflows on the 1024th pulse, at which time the Program Loop Counter is incremented. The entire process is then repeated until the required number of program puses has been received by each PROM location, and the Program Loop Counter overflows, resetting the Program Cycle Latch. The PROM can now be read or verified by way of the PROM cycle request.

To modify data in a partially programmed PROM it is only necessary to read the PROM into the RAM, enter the new data pattern, and check to be sure that no bits will be attempting to program 0's to 1's, and reprogram the PROM as described above. The only method of programming a "1" where there is a "0" is to erase the entire device and reprogram. This process is illustrated graphically in Figure 12.

STATUS	PROM OUTPUTS							
	O_1	O_2	O_3	O_4	O_5	O_6	O_7	O_8
INITIAL STATE	1	1	1	1	1	1	1	1
FIRST PROGRAMMING	1	1	0	0	1	0	1	0
FIRST REPROGRAMMING	0	1	0	0	0	0	1	0
SECOND REPROGRAMMING	0	0	0	0	0	0	1	0
FINAL REPROGRAMMING	0	0	0	0	0	0	0	0
ERASURE	1	1	1	1	1	1	1	1

Figure 12. Reprogramming 2708 Outputs

Program Pulse Driver Circuits

Figure 13 presents several circuits which have been successfully used to generate the required 26V pulse for programming, and one circuit which should not be used.

The circuit shown in Figure 13a should not be used, as the resistive pull-down will not meet the V_{ILP} requirement of 1V max, thus not allowing $V_{IHP}-V_{ILP}$ to be equal to or greater than 25V. As was mentioned earlier, the reason for this is that the Program pin, Pin 18, sources I_{ILP} of about 2 mA when the program pulse is low and $\overline{CS}$/WE is at +12V. The other circuits, b and c, do meet all the A.C. and D.C. specifications associated with the program pulse.

$\overline{CS}$/WE Driver Circuits

Figure 14 presents several circuits for generating the $\overline{CS}$/WE signal. Circuit a is very simple, providing the three necessary levels for on board programming. Circuit b has increased driving capability and isolation over circuit a, and will allow more noise margin. In addition, the inclusion of the two 100Ω resistors provide short circuit protection in case of socketing or soldering errors. A truth table is included with circuits a and b to indicate the various input/output conditions. Circuit c provides only two levels, V_{IL} (0V) and V_{IHW} (+12V), for use in "program and verify only" circuits; the PROM cannot be deselected using this circuit. Another way of generating the 0 and +12V signals would be to use a TTL to MOS driver, such as the Intel® 3245.

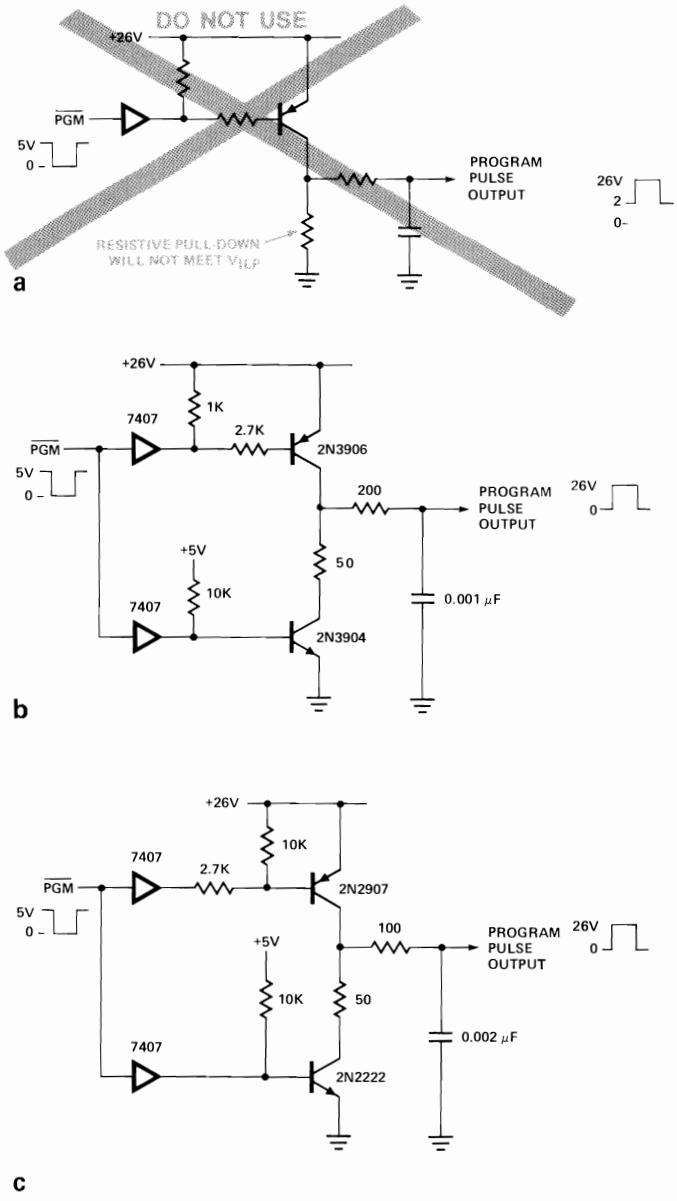
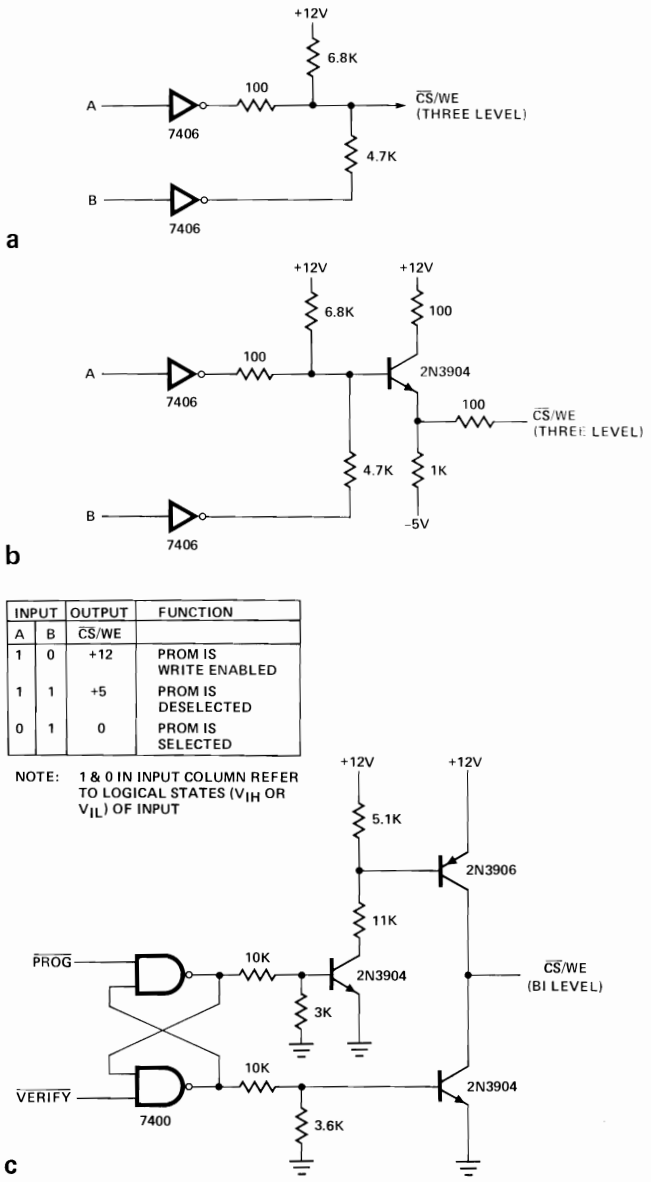


Figure 13. Program Pulse Driver Circuits



INPUT		OUTPUT	FUNCTION
A	B	$\overline{CS}$/WE	
1	0	+12	PROM IS WRITE ENABLED
1	1	+5	PROM IS DESELECTED
0	1	0	PROM IS SELECTED

NOTE: 1 & 0 IN INPUT COLUMN REFER TO LOGICAL STATES (V_{IH} OR V_{IL}) OF INPUT

Figure 14. $\overline{CS}$/WE Driver Circuits

On Board Programming

Unlike many other erasable and programmable Read Only Memories, the 2708 can be soldered directly into a printed circuit board and programmed while "in circuit", as the inputs and outputs stay low level compatible during both read and program modes of operation. When erasure is required, the circuit board is unplugged and placed under a UV lamp for the required period of time.

In many microprocessor systems, it is quite easy to implement the RAM storage required for a data base when programming by using available RAM storage. Be sure to observe all the required setup times if the address and data bus will be performing non-programming related functions while the PROM is being programmed.

Figure 15 illustrates a possible scheme for implementing a data output/input buffer.

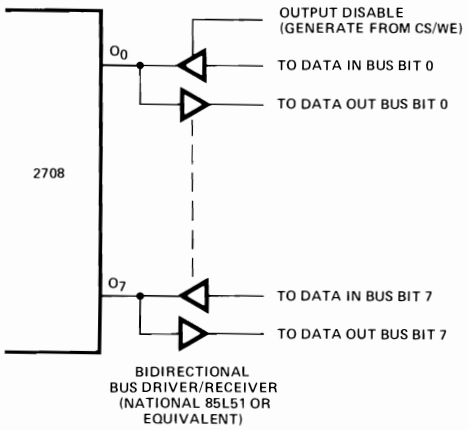


Figure 15. Data Output/Input Buffer

To take advantage of this feature, which is not tested or included as part of the device specifications, the program pulse should be applied to all devices as shown in Figure 16. Program decode is then accomplished by way of the $\overline{CS}$/WE pin. PROM's to be programmed have this pin raised to the V_{IHW} level (+12V), while it is left at V_{IH} ($\overline{CS}$=3V) for those parts which are not to be programmed. Reserve should be built into the program pulse power supply when operation in this mode is planned, but in no case will it exceed the maximum of 20 mA per 2708 as specified in Table III.

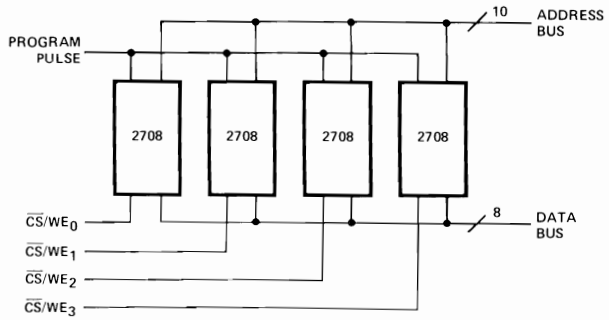


Figure 16. Circuit Implementation for On-Board Programming

ERASING

The 2708 is erased by exposure to ultra-violet light at a wavelength of 2537Å. The recommended integrated dosage (i.e. UV intensity X exposure time) is 10 W-sec/cm^2. In order to insure that all bits are erased, this dosage includes a guard band and is not equal to the dosage required to see the last bits return to the initial state. A guard band of 3 to 4 times the initial period (that time which appears to erase all bits) is suggested so that the device will appear erased at extremes of temperature and voltage.

Table V. UV Sources for Erasing the 2708

Model	Power Rating	Typical Time to Erase a 2708 Device
S-68	12000 uW/cm^2	10 minutes
S-52	12000 uW/cm^2	10 minutes
UVS-54	5700 uW/cm^2	30 minutes
R-52	13000 uW/cm^2	10 minutes
UVS-11	5500 uW/cm^2	30 minutes

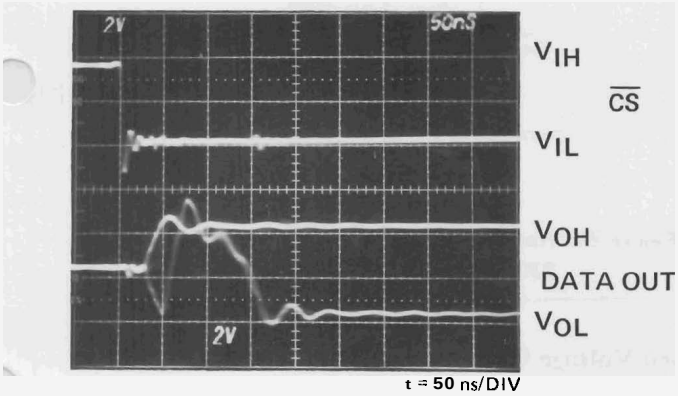
Table V lists several UV sources for erasing the 2708. The model numbers referred to are manufactured by Ultra-Violet Products, Inc. (5114 Walnut Grove Avenue, San Gabriel, CA).

The times indicated are for the lamps placed about 1 inch away from the parts to be erased and without shortwave filters installed. For lamps other than those listed, the required times can be determined empirically or by means of an ultra-violet intensity meter, such as the UV Products Model J-225. When a meter is used, the intensity should be determined at the same location (distance from UV tube) as the PROM will be placed; this will require careful measurement to insure that the sensor is receiving exactly the same amount of UV light that the PROMs will receive.

APPLICATIONS

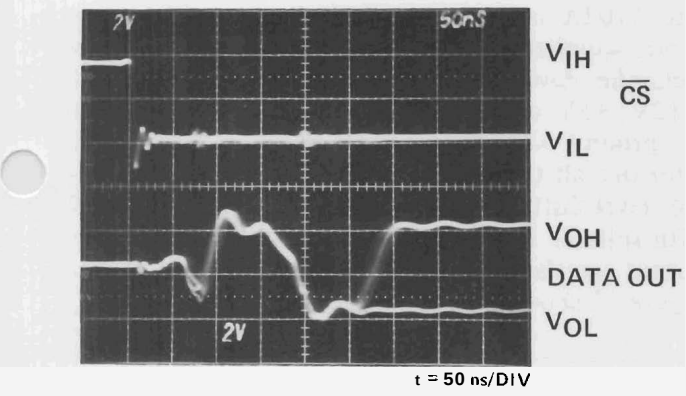
Switched Power Supplies

Although not specified in the D.C. and A.C. DEVICE SPECIFICATIONS sections, the 2708 can be operated in a power down mode by switching off the V_{DD} power supply. This is advantageous in many applications where power dissipation is a critical factor, such as battery operated or battery backed-up systems. Referring to Table II, the maximum I_{DD} power that can be saved by switching the V_{DD} power supply is 780 mW. Two factors should be noted, however. First of all, the access time will increase somewhat, as shown in Figure 17.



t = 50 ns/DIV

a. WITHOUT SWITCHED V_{DD}



t = 50 ns/DIV

b. WITH SWITCHED V_{DD}

Figure 17. 2708 Access Time

The photos were taken using the circuit of Figure 18, at room temperature and with a small sample of parts. Based on this information, the PROM data strobe should be moved out approximately 150 ns to allow a guard band for the system. The second point related to the switching of V_{DD} is the reduction of V_{BB} current (I_{BB}). Figure 19 indicates that I_{BB} decreases to an average of approximately 8 mA when V_{DD} is off.

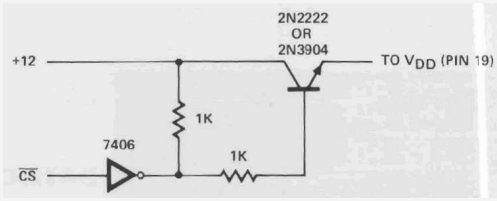
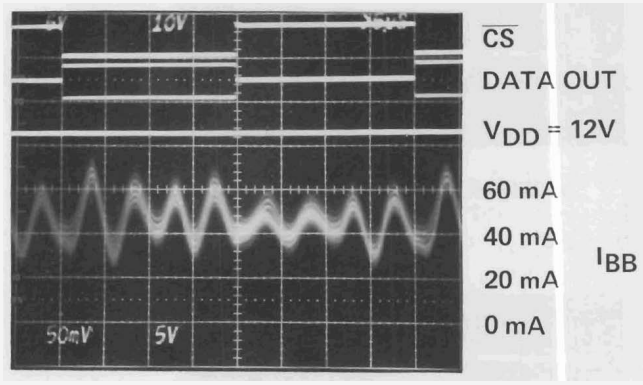
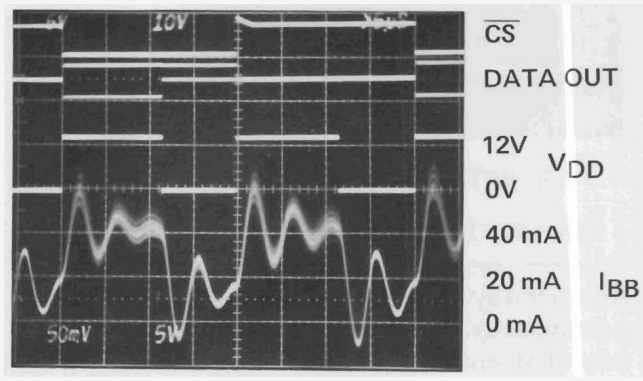


Figure 18. Circuit for Switching V_{DD}



a. WITHOUT SWITCHED V_{DD}



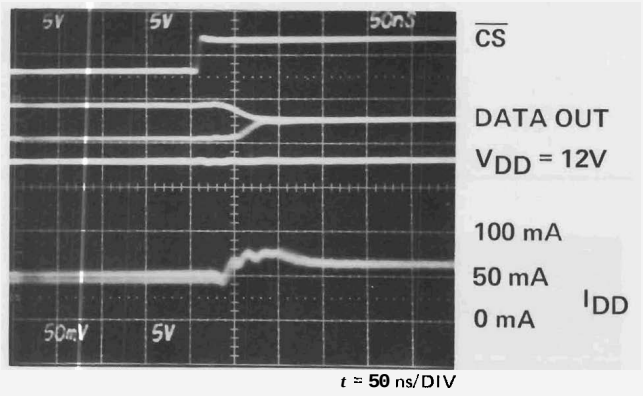
b. WITH SWITCHED V_{DD}

Figure 19. 2708 I_{BB} Current

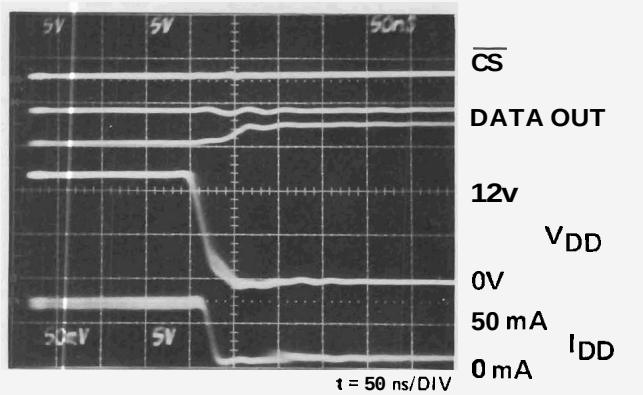
As shown in Figure 20, output deselection occurs within t_{DF} (Chip Select to Output Float Delay) when $\overline{CS}$ is held low and V_{DD} is switched.

Switching off V_{CC} will save some power, but the maximum value is so low (10 mA) that the extra components required for switching are probably not justified. Typical values of I_{CC} decrease about 50% when the V_{DD} supply is switched off.

The V_{BB} supply could also be switched, but, considering the reduction when the V_{DD} supply is switched off, the additional components required to switch this supply would probably not be justified, either. In addition, unless an extra power supply of −10 to −15 volts is available for a driver circuit, access time would be significantly degraded (laboratory data indicates about 50 μs).



a. WITHOUT SWITCHED V_{DD}



b. WITH SWITCHED V_{DD}

Figure 20. 2708 Output Deselection and I_{DD} Current

Another way of reducing power is to leave the device continuously selected and control the output by way of an enable signal on a latch or gate. Referring to Figure 8, this method would reduce power dissipation nearly 50%, as the device does dissipate less power when $\overline{CS}/WE$ is low.

OR Tie Considerations

When two or more 2708's are wire ORed together, care should be exercised to see that valid data will be obtained. Referring back to Figure 7 and Figure 21, if two devices are selected at the same time, a current path can exist from Q_1 to Q_4 is shown in Figure 21. This current can be destructive to the output stage of one of the devices, or, the transistor with greater current sourcing or sinking capability can cause false data to be read from the output bus. In addition, the very high V_{CC} current drawn while both Q_1 and Q_4 are on will generate noise on the V_{CC} power supply lines, and possibly reduce the V_{CC} that is connected to other TTL control circuits, causing momentary false indications. If the maximum chip deselect to output float delay (t_{DF}) is observed, there will be no problem. The same type of situation can occur when the 2708 is used in conjunction with other memory devices, such as the RAM portion of the programmer shown in Figure 11. Careful analysis of the system timing requirements and maximum delay paths can eliminate these problems before they occur at the final checkout of a system.

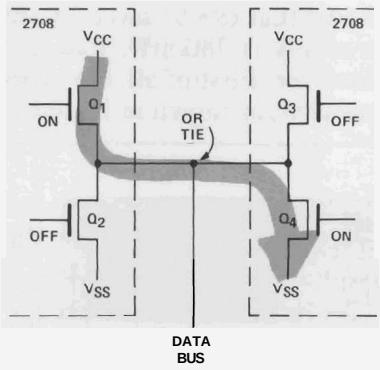


Figure 21. Results of Improper Timing when OR Tying 2708's

High Voltage CMOS Interface

Because the 2708 is erased by the same technique as the Intel® 1702A, some users have assumed that the various techniques for interfacing to high voltage CMOS circuits are similar. In fact, they are not. The 1702A is a p-channel device, requiring two power supplies (+5V and –9V), while the 2708 is a n-channel device and requires three power supplies (+12V, +5V and –5V). It is permissible to assign the ground (OV) to the most negative supply and reference all the other supplies to it; however, suitable level shifters must be used to provide the 2708 with suitable input level signals, and to convert the output signals back to the system reference levels. Figure 22 shows a possible voltage translation.

SUPPLY	2708 VOLTAGE	SYSTEM VOLTAGE
V_{DD}	+12V	+17V
V_{CC}	+ 5v	+10V
V_{SS}	OV	+ 5v
V_{BB}	- 5V	0V
V_{IL}	0 to +0.65	+5.0 to +5.65
V_{IH}	+3.0 to +6.0	+8.0 to +11.0
V_{OL}	+0.45	+5.45
V_{OH}	+2.4 @ –1 mA	+7.4

Figure 22. 2708 Voltage Translation

Some suitable translator circuits arc: RCA CD4009/4010 or National F/4104/34104. The use of these circuits also allows some high voltage **CMOS** logic to be implemented, such as address and data clocks, at the **CMOS** levels, rather than convert them to TTL levels for operation of the 2708.

Another incorrect method of attempting to interface directly to **CMOS** circuits is to change the V_{CC} supply to the new interface voltage. In devices such as the Intel® 2107B this is permissible, as the V_{CC} supply is connected to the output buffer stage, but in the 2708, the +5V is used in the sense amplifier and other internal circuitry, so this should not be done.

Under Programming and Under Erasing

It is possible to "under program" the 2708, such that the cell characteristic crosses the sense threshold. The result of this is that the cell apparently drops or picks up bits. As can be seen in Figure 33, the threshold characteristic has been shifted such that small changes in voltage or temperature will cause a "1" or a "0" to be sensed. This is always the result of insufficient erasing or programming. For erasure to cause this problem, the device has only been partially programmed, and the characteristic curve has only been shifted to the sense threshold point and the device will again seem to either pick up or drop bits. The cure, in either case, is to 1) adequately erase by providing the required 10 W-sec/cm^2 of UV light at a frequency of 25378, or 2) program in accordance with the specifications.

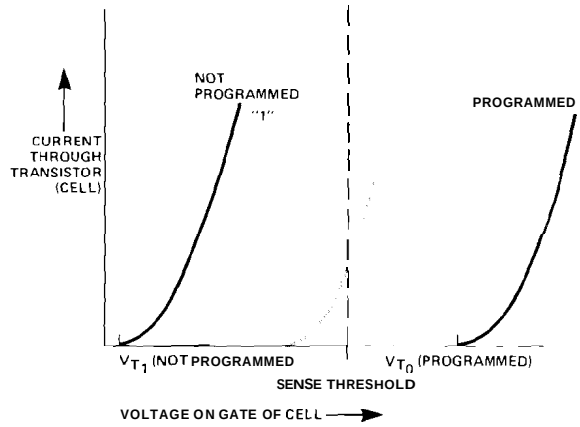


Figure 23. Effect of Under Programming or Under Erasure

ACKNOWLEDGEMENT

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