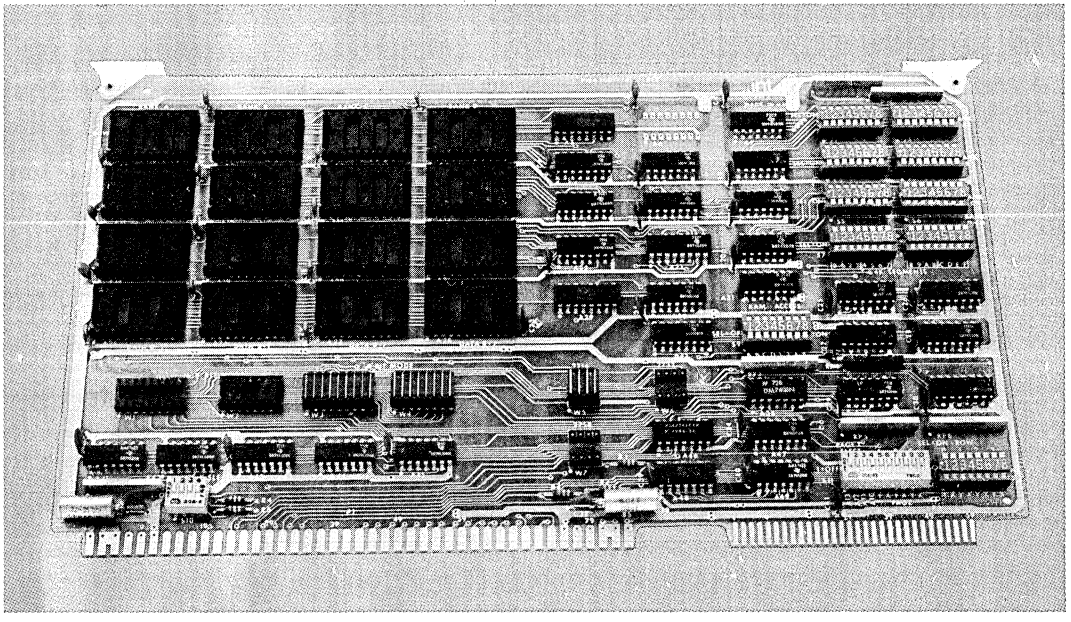
iSBC™ 464
64K BYTE EPROM EXPANSION BOARD

- **Provides EPROM/ROM expansion of iSBC™ 80, iSBC™ 86 and iSBC™ 88 systems via direct MULTIBUS interface**
- **Sockets for up to 64K bytes of EPROM**
- **Compatible with Intel® 2758, 2716 or 2732/2732A erasable PROMs**
- **Switch selectable base address on 4K byte boundaries for each memory bank**
- **Assignable anywhere within a 1 megabyte address space**
- **EPROM components which are not enabled are placed in standby power mode**
- **Requires a single +5V power supply**

The iSBC 464 is a member of Intel's complete line of iSBC memory and I/O expansion boards. The iSBC 464 board interfaces directly to the iSBC 80, iSBC 86 or iSBC 88 single board computers via the MULTIBUS system bus, to expand system EPROM memory capacity.



FUNCTIONAL DESCRIPTION

Memory Configuration

The iSBC 464 board contains sixteen sockets which provide a maximum of 64K bytes of memory expansion. The actual capacity of the board is determined by the type and quantity of EPROM components installed by the user. The board is compatible with three different sizes of Intel EPROM devices. These are the 1K byte 2758 EPROM, the 2K byte 2716 EPROM, and the 4K byte 2732 EPROM.

Mode of Operation — The iSBC 464 board can operate in one of two modes: the 8 bit only mode or the 16/8 bit mode. The 8 bit mode provides the most efficient memory configuration for systems handling 8 bit data. The 16/8 bit mode allows 16 bit words to be accessed by 16 bit processors. In the 16/8 bit mode, 16 bit and 8 bit microprocessors may also access either the high order byte or the low order byte of a 16 bit word. The mode of operation is selected by placing two option jumper blocks in the appropriate sockets.

Memory Banks — When used in the 8 bit mode, the iSBC 464 board is organized into four banks (labeled A-D) of four sockets each. Depending on the type of memory components used, each bank may contain a maximum of 4K, 8K or 16K bytes of memory. Unused memory sockets may be deselected by bank or individually in bank D. Deselecting a bank or individual socket frees that address space for use elsewhere in the system. In the 16/8 bit mode, banks A & B and C & D are paired together to form two banks (labeled AB, CD) which are 16 bits wide. Each of these banks has four socket pairs. Bank AB may be deselected as a single unit. Socket pairs in bank CD may be deselected individually. Thus, board configurations using fewer than 16 memory components do not fill memory address space with unused sockets. Selection/deselection is accomplished by setting switches on the board.

Memory Access Time — The iSBC 464 board operates with one of 15 switch selectable memory access times ranging from 35 to 1435 nanoseconds. This feature allows the board to be tailored to the performance of the installed components and the system CPU.

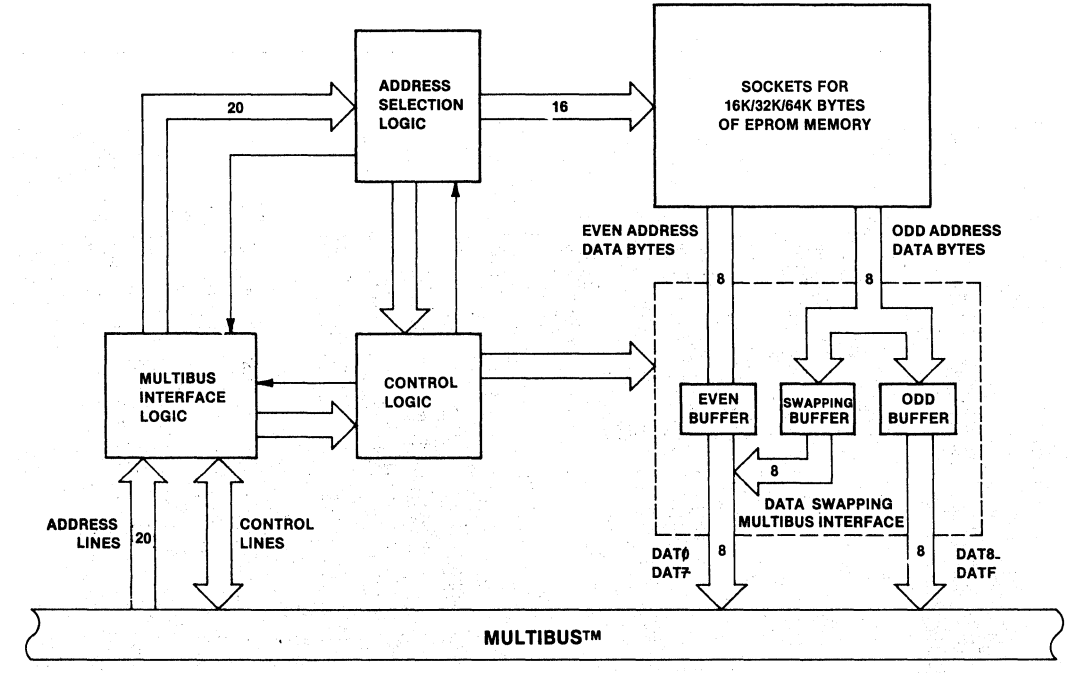


Figure 1. iSBC 464 Block Diagram

Memory Addresses

Switch selectable options on the iSBC 464 board allow the board to be assigned anywhere within a 1 megabyte address space. In either operating mode, the base address of each memory bank may be set to any 4K byte boundary within a 64K byte memory page. There is one exception. If the 4K byte devices are used in the 16/8 bit mode, then base addresses are restricted to 8K byte boundaries. If the board is used in a system with an address range greater than 64K bytes, memory on the iSBC 464 board may reside in one or two 64K byte memory pages. Any two pages out of a possible 16 may be chosen by setting switches on the board.

Standby Power Operation

The iSBC 464 board takes advantage of the standby modes of the Intel 2758, 2716 and 2732. When they are not enabled, these components draw as little as 25% of their active level power with no degradation in access time. The iSBC 464 board is designed so that only two memory components are enabled during a read operation.

RAM Overlap

Memory banks of the iSBC 464 board can be overlapped with the addresses of system RAM by setting on-board switches. The process of addressing a memory bank will drive the Inhibit RAM (INH1/) signal true. This signal is issued to the MULTIBUS system bus in order to prevent any MULTIBUS accessable RAM in the system from responding to the current address. If an EPROM is addressed which has its corresponding RAM overlap switch on, an access time of 15 clock cycles is imposed. This allows overlapped dynamic RAM to refresh before the address on the MULTIBUS is changed. The RAM overlap feature does not apply to RAM which is not on the MULTIBUS system bus.

SPECIFICATIONS

Word Size

8 bits or 16 and 8 bits

Memory Size

Sockets are provided for up to 16K bytes in 1K increments or 32K bytes in 2K increments or 64K bytes in 4K increments

Compatible Intel® Memory

EPROM — 2758 or 2716 or 2732

INTERFACE — All 20 address, 16 data, and 6 control signals are TTL compatible and Intel MULTIBUS compatible

Electrical Characteristics

DC Power (max)

V_{CC}: +5V DC ±5%
I_{CC}: 1.1 amps without EPROMs
I_{CC}: 1.6 amps with (16) 2716s or 2758s
I_{CC}: 1.3 amps with (16) 2732s or 2732As

Connectors

Bus — 86-pin double-sided PC edge connector with 0.40 cm (0.156 in.) contact centers

Mating Connector — Viking 3KH43/9AMK12 or compatible connector

Physical Characteristics

Length — 30.48 cm (12 in.)
Height — 17.15 cm (6.75 in.)
Depth — 1.27 cm (0.5 in.)
Weight — 294 gm (10.5 oz) without EPROM

Environment

Operating Temperature — 0°C to +55°C
Relative Humidity Limits — <90% non-condensing

Reference Manual

9800643A — iSBC 464 Memory Expansion Board Hardware Reference Manual (NOT SUPPLIED)

Manuals may be ordered from any Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

Part Number	Description
SBC 464	64K EPROM Expansion Board