i960® Processor
Assembler User's Guide

Order Number: 485276-006

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Contents

Chapter 1  Overview
What's New in the Assembler for CTOOLS 6.0 ................. 1-1
i960® Processor Assembler and Related Tools ................. 1-1
Compatibility and Standards .............................................. 1-2
About This Manual ............................................................. 1-3
    Target Audience .......................................................... 1-3
    Conventions ................................................................ 1-3
Customer Service .............................................................. 1-5

Chapter 2  Writing Assembly Language Code
for the i960 Rx Processor
Introduction ........................................................................ 2-1
    What is the “Rx Strategy?” ........................................... 2-1
    How Do I Use the Rx Strategy? ................................... 2-1
    How Do I Use the Jx-Specific Strategy? ....................... 2-2
    How Do I Decide Which Strategy to Use? ................. 2-2
    Writing Assembly Code With the Rx Strategy ............ 2-3
    Writing Assembly Code Without the Rx Strategy ....... 2-4
Details of the Rx Strategy .................................................. 2-4
    80960 Instruction Set Support ................................... 2-4
    Big-Endian Support ..................................................... 2-7
    b.out OMF Support ..................................................... 2-7
    80960 Assembly Language Converter (xlate960) .......... 2-8
Improved Assembler Pseudo-instruction Support .......... 2-8
    Introduction ............................................................... 2-8
Chapter 3 Invoking the Assembler
Invocation Command ......................................................... 3-1
   Specifying Option Arguments .................................... 3-2
   Specifying Single and Multiple Options ...................... 3-2
   Using Uppercase and Lowercase ................................ 3-3
   Naming the Object File .............................................. 3-4
   Providing Source Input ............................................... 3-5
Environment Variables ...................................................... 3-6
   Selecting the Instruction Set and Libraries .................. 3-7
   Defining a Base Directory Path .................................. 3-8
   Defining an Identification String ............................... 3-8
   Redirecting Error and Warning Message Output .......... 3-8
   Building a Search Path for Include Files .................... 3-8
   Building the Search Path for the Assembler Executable  3-9

Chapter 4 Option Reference
A: Architecture .............................................................. 4-3
D: Define symbol ......................................................... 4-4
d: Debug symbols ....................................................... 4-6
G: Big-endian target ...................................................... 4-7
I: Include-file search path ............................................ 4-8
i: Input from stdin ...................................................... 4-9
L: Generate a listing ...................................................... 4-10
n: No compare-and-branch replacement ....................... 4-16
o: Object filename ....................................................... 4-17
p: Position independence ............................................. 4-18
t: Translate ............................................................... 4-19
V, v960: Version .......................................................... 4-20
W: Warnings ............................................................... 4-21
Contents

x: Allow mixed architectures .............................................. 4-21
z: Time stamp .................................................................... 4-23

Chapter 5  Directives
Syntax ............................................................................... 5-2
Specifying the Input ........................................................... 5-3
Controlling the Location Counter........................................ 5-3
  Setting the Location Counter to a Specific Value........... 5-3
  Moving the Location Counter to a Section............... 5-4
Initializing Data .................................................................. 5-5
  Initializing Byte, Ordinal, and Integer Data ............... 5-6
  Initializing Floating-point Data ................................. 5-6
  Initializing String Data................................................. 5-6
Initializing Blocks of Memory.............................................. 5-7
Defining Symbols............................................................... 5-7
Providing Debugger Information ........................................ 5-8
Optimizing.......................................................................... 5-9
Marking Position Independence......................................... 5-10
Controlling the Listing ........................................................ 5-10
Directives Reference ......................................................... 5-10

Chapter 6  Messages

Chapter 7  Assembly Language
Assembly Language Statement Format......................... 7-1
Character Set ................................................................. 7-2
Tokens and Separators...................................................... 7-3
Identifiers ........................................................................... 7-3
Constants ............................................................................. 7-3
  Simple Constants ............................................................. 7-3
  Representing Floating-Point Numbers......................... 7-4
  Character Constants ....................................................... 7-5
  String Constants............................................................ 7-6
Labels ................................................................. 7-6
  Name (Global) Labels ............................................ 7-7
  Numeric (Local) Labels ........................................ 7-7
Expressions .......................................................... 7-7
  Operators ............................................................ 7-8
  Expression Types .................................................. 7-10
  Type Propagation in Expressions ............................ 7-13
Comments .............................................................. 7-14
Summary of Core Instructions ................................. 7-15
  Data Movement ..................................................... 7-15
    Load ................................................................. 7-16
    Store ............................................................... 7-16
    Move ............................................................... 7-17
    Select ............................................................. 7-17
Ordinal and Integer Arithmetic ............................... 7-18
  Basic Arithmetic ............................................... 7-18
  Extended Arithmetic .......................................... 7-19
  Conditional Arithmetic ....................................... 7-19
  Remainder and Modulo ....................................... 7-21
  Shift and Rotate ................................................ 7-21
Logical ................................................................. 7-22
Bit, Bit Field, Byte .............................................. 7-24
  Bit Operations ................................................... 7-24
  Bit Field Operations ......................................... 7-25
Byte Operations .................................................. 7-25
Comparison ......................................................... 7-25
  Compare and Conditional Compare ....................... 7-26
  Compare and Increment or Decrement .................... 7-27
Branch ................................................................. 7-27
  Unconditional Branch ............................................ 7-28
  Conditional Branch ............................................. 7-28
  Compare and Branch ........................................... 7-29
Call and Return .................................................... 7-30
Fault ................................................................. 7-31
Debug ............................................................... 7-32
Processor Management ......................................... 7-32
Synchronous (K-series only) .................................... 7-34
Atomic ............................................................... 7-35
Summary of On-chip Numerics Instructions ............... 7-35
  Data Movement .................................................. 7-35
  Sign Copying .................................................... 7-37
  Data Type Conversion ....................................... 7-37
  Basic Arithmetic .............................................. 7-38
  Decimal .......................................................... 7-39
  Comparison and Classification .............................. 7-40
  Trigonometric Functions .................................. 7-41
  Logarithmic, Exponential, and Scale ..................... 7-42

Chapter 8 Pseudo-instructions
Syntax .................................................................... 8-1
Branch Pseudo-instructions ..................................... 8-2
Migration-enabling Pseudo-instructions .................... 8-2
Conditional Faults Pseudo-instructions ..................... 8-4
Load Pseudo-instructions ...................................... 8-4
Call Pseudo-instructions ....................................... 8-4
Compare-and-jump Pseudo-instructions .................... 8-4
Pseudo-instructions Reference ............................... 8-7
Chapter 9 Example Programs

Examples Using the Core Instruction Set ...................................... 9-1
  Enable and Count Interrupts From 8259A ......................... 9-2
  Send an IAC to the Processor ........................................... 9-8
  Perform a BitBlt Operation ............................................ 9-9
  Perform Matrix Multiplication ......................................... 9-11
  Compare Strings ......................................................... 9-13

Examples Using Floating-point Instructions ......................... 9-14
  Optimize a Numerics Application .................................. 9-14
  Perform Matrix Multiplication ....................................... 9-16
    Assembly Code .................................................... 9-16
    C Code ............................................................. 9-18
  Perform Basic Numerics Operations ................................ 9-19
  Exponentiate With an Arbitrary Exponent ......................... 9-19
  Convert Between Coordinate Systems ................................ 9-20
  Retrieve Fault Record Pointer ...................................... 9-21

Glossary

Index

Examples

  7-1 Example of Constants and Literal Values .................. 7-5
  7-2 Forward-reference External Symbol in Expressions .... 7-8
  7-3 Example of Register Usage ..................................... 7-13

Figures

  9-1 IAC Message Structure ......................................... 9-8
  9-2 Stack For Fault Handler ........................................ 9-21
Contents

Tables

2-1 New Assembler Pseudo-Ops ..................................... 2-9
3-1 Assembler Environment Variables ............................ 3-7
4-1 Assembler Options .............................................. 4-1
4-2 CORE0-3 Architecture Compatibilities .................... 4-4
5-1 Functions Performed by Directives ......................... 5-1
7-1 Assembly Language Character Set ............................ 7-2
7-2 Prefixes for Floating-point Constants ...................... 7-4
7-3 Floating-point Literals ....................................... 7-5
7-4 Character Constants ......................................... 7-6
7-5 Expression Operators ........................................ 7-9
7-6 Operator Precedence ......................................... 7-9
7-7 Predefined Register Symbols ................................ 7-12
7-8 Unary Operation ............................................... 7-23
7-9 Binary Operations ........................................... 7-23
7-10 Binary Operations Continued ............................... 7-23
7-11 Supported Processor Management Instructions .......... 7-33
8-1 Branch Real Pseudo-instructions ......................... 8-2
8-2 New Assembler Pseudo-Instructions ...................... 8-3
8-3 Compare-and-jump Pseudo-instructions .................. 8-6
8-4 Breakpoint Resource Status Word Bits .................. 8-10
8-7 Compare and Jump Substitutions .......................... 8-18
8-8 Data Cache Status Word Bits .............................. 8-20
8-9 Instruction Cache Status Word Bits ....................... 8-24
Overview

This chapter of the i960® Processor Assembler User’s Guide introduces you to the i960 processor assembler and to this manual.

This chapter describes:
- new features in the assembler
- using the assembler with other i960 processor software tools
- the standards and conventions used by the assembler and in this manual
- the trademarks and copyrights pertaining to this manual

What’s New in the Assembler for CTOOLS 6.0

This release features enhanced support for developing assembly language code for the Intel i960 Rx processor. This includes:
- Writing assembly language code for the i960 Rx processor.
- xlate960, 80960 assembly language translator
- Improved pseudo-instruction support for gas960/asm960

See Chapter 2 for information on these topics.

i960® Processor Assembler and Related Tools

The i960 processor assembler is part of a complete set of software and hardware tools for developing embedded applications for the i960 processors. Use ic960 or gcc960, the i960 processor assembler, and the i960 processor software utilities to translate, link, and format source text into executable or PROM-programmable code. You can write assembly source text directly in a text editor or compile a C/C++ program to produce assembly output. To create object files, you can assemble your source text
or the assembly output from the C/C++ compiler. Disassembled text from
the dumper is for debugging only and cannot be reassembled. For more
information on how the software tools work together, see the Getting
Started manual.

Compatibility and Standards

The assembler described in this manual supports the i960 Sx, Kx, Cx, Jx,
Hx, and Rx processors.

The assembler accepts output from Release 3.0 and later of the
CTOOLS960 compiler and from Release 1.2 and later of the GNU/960
compiler.

You can specify the assembler object file output format as either
common object file format (COFF), b.out or ELF format. The output
format depends on the assembler invocation command, as shown:

• For b.out format, invoke the assembler with the gas960 command.
• For COFF format, invoke the assembler with the gas960c or asm960
  command.
• For ELF format, invoke the assembler with the gas960e command.

For backwards compatibility with your existing script or batch files, the
directory structures and search paths used by the assembler depend on the
invocation name, as shown:

• For behavior similar to the GNU/960 (Release 1.2 or later) assembler,
  invoke the assembler with gas960, gas960c, or gas960e.
• For behavior similar to the CTOOLS960 (Release 3.5) assembler,
  invoke the assembler with asm960.

Note that when you invoke the assembler as asm960 you can generate the
COFF output format only.
About This Manual

This manual, the *i960 Processor Assembler User's Guide*, is part of the i960 processor software development tools manual set. See *Getting Started with the i960 Processor Software Development Tools* for a list of all manuals in the i960 processor development tools library.

The *i960 Processor Assembler User's Guide* provides operating instructions for the assembler. This manual does not teach development techniques.

Target Audience

To use the assembler effectively, you must be familiar with the i960 architecture and the development process.

This manual does not provide detailed information about the target processor. The processor manuals listed in *Getting Started with the i960 Processor Software Development Tools* contain information such as:

- a description of the i960 architecture
- the processor theory of operation and descriptions of the on-chip devices
- information about low-level programming for particular processors

For additional information about these topics, order the relevant publications listed in *Getting Started with the i960 Processor Software Development Tools*.

Conventions

In addition to the standard typographical conventions listed on the front inside cover, this manual uses the following notation and format conventions.

Case is significant for directives, functions, options, and option arguments. On UNIX*, case is also significant for invocation names and filenames.
Arguments and operands are in italics. The operand names indicate the function of the operands (for example, *filename*, *expr*).

Directive and pseudo-instruction operands use the following notation:

- **addr** represents an address.
- **align** represents an exponent of 2, used as an alignment factor.
- **data** represents ordinal, integer, or floating-point data; the format of the data depends on the instruction or directive.
- **int** represents a positive integer.
- **name** represents a symbol or label.
- **size** represents an integer, used as a size factor.
- **string** represents a sequence of ASCII characters.
- **expr** indicates an expression.

Special characters, delimiters, and other punctuation used with the operands, such as quotation marks and commas, are explicitly shown.

Notation for registers is one or more letters indicating the kind of register and a number between 0 and 15, as follows:

- **global register** a register g0 through g14, and fp.
- **local register** a register pfp, sp, rip, and r3 through r15.
- **special function register** a register available only on the i960 Cx and Hx processors: sf0–sf2 (Cx) and sf0–sf4 (Hx).
- **floating-point register** a register available only with on-chip floating-point support: fp0, fp1, fp2, and fp3.

For more information on the registers, see the processor manuals listed in *Getting Started with the i960 Processor Software Development Tools*. 
Target expressions \((\text{targ})\) representing a memory address are assembled as a signed displacement value representing an IP-relative address:

<table>
<thead>
<tr>
<th>Format</th>
<th>Displacement</th>
<th>Target (targ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>COBR</td>
<td>(-2^{10} : 2^{10}\cdot1)</td>
<td>(-2^{12} : 2^{12}\cdot4) from IP</td>
</tr>
<tr>
<td>CTRL</td>
<td>(-2^{21} : 2^{21}\cdot1)</td>
<td>(-2^{23} : 2^{23}\cdot4) from IP</td>
</tr>
</tbody>
</table>

For convenience in cross-referencing material, the notation used in the reference sections follows that of the processor manuals listed in \textit{Getting Started with the i960 Processor Software Development Tools}.

**Customer Service**

If you need service or assistance, see \textit{Getting Started with the i960 Processor Software Development Tools}.
Introduction

This chapter provides information on designing assembly language code for use with the i960 Rx family of microprocessors, including the RP and RD processors. It describes the two possible paths to follow in designing assembly-language solutions for i960 Rx processors. The first of these paths is the “Rx Strategy”, designed to ease transition to i960 Rx processors beyond the RP and RD. The other path is the “Jx-Specific Strategy”, designed specifically for Rx processors that are based on the i960 Jx core (such as the RP and RD) and providing maximum low-level processor control.

What is the “Rx Strategy?”

The “Rx Strategy” refers to a set of CTOOLS enhancements implemented to help you move from existing i960 RP and RD processors to possible future implementations of the i960 Rx family. CTOOLS added the new -ARP and -ARD architecture switches, which allow only those instructions that are most likely to be supported on future i960 Rx processor offerings. In addition, CTOOLS provides enhancements that have no effect on today’s i960 Rx processors, but that may be used on future processors.

How Do I Use the Rx Strategy?

Using the Rx strategy is as simple as specifying the -ARP or -ARD option when invoking the CTOOLS utilities. (You can also set the $I960ARCH or $G960ARCH environment variables to RP or RD.)
How Do I Use the Jx-Specific Strategy?

If you decide not to follow the Rx strategy, use the -AJF architecture option when creating code for use with i960 RP and RD processors. For information on specific differences between the -ARx switches and the -AJF switch, please see Details of the “Rx Strategy”. For help deciding if the Rx strategy is the best choice for your application, please read the next section.

How Do I Decide Which Strategy to Use?

Use these questions to help you decide which of the two development paths you should follow:

- **How important is backward-compatibility with other i960 core processors (e.g., KA, CF, JF)?** If you have legacy code that you wish to use with the i960 Rx processors, you may want to use the -AJF switch. Doing so gives you the most flexibility in terms of available instructions and addressing modes.

- **How important is forward-compatibility with future i960 processors?** If you wish to minimize the effort involved in moving to future Rx processors, you should use the Rx strategy.

- **Will you be writing my applications from scratch?** When writing new applications, follow the Rx strategy when possible. Tests have shown that there is seldom a significant performance or code size penalty, and you may actually see an improvement in either area.

- **How much low-level processor access do you need?** If you need access to low-level processor resources such as the PC (Process Control) or TC (Trace Control) registers beyond that provided in the updated assembler pseudo-instructions (see Improved Assembler Pseudo-instruction Support for gas960/asm960), you cannot use the Rx strategy.

Based on your answers to the questions above, you should now be able to decide which path to follow: the Rx strategy or the Jx-specific strategy. After you make your decision, read the corresponding section below for specific tips on making the most of your programming environment. If
you choose to follow the Rx strategy, please read *Writing Assembly Code With the Rx Strategy*. If you choose to follow the Jx-specific strategy, please read *Writing Assembly Code Without the Rx Strategy*.

**Writing Assembly Code With the Rx Strategy**

To take advantage of CTOOLS enhancements supporting the Rx strategy, simply use the Rx architecture switches (e.g., `-ARP`, `-ARD`) for all applicable CTOOLS applications. You can also set the $I960ARCH or $G960ARCH environment variables to RP or RD. If you are migrating code written for other i960 core processors (e.g., KA, CF, HA), you can use xlate960, the 80960 translation utility as a starting point for your migration. The translator generates Rx-compatible code sequences to replace instructions and addressing modes that appear in the JF processor but not the Rx strategy. See *xlate960, 80960 Assembly Language Translator* for information on using this application.

If you need to use some of the JF-specific features not supported in the Rx strategy, such as disabling interrupts, cache control, or atomic accesses, you can use the new assembler pseudo-instructions. The primary benefit of using these instructions is that they should not require modification when assembled for future i960 Rx processors. Information on these new pseudo-instructions is available in *Improved Assembler Pseudo-instruction Support for gas960/asm960*. Note that if you use any of the new i960 processor pseudo-instructions you are required to re-assemble your source before running it on i960 Rx processors that are not based on the i960 JF core. This is because the instruction sequence generated for the new pseudo-instructions is not guaranteed to be compatible with future Rx processors.

Finally, specific information on the architectural implications of the `-ARP` and `-ARD` switches are in *Details of the Rx Strategy*. 
Writing Assembly Code Without the Rx Strategy

To write code that is designed for i960 JF-based Rx processors only, use the JF architecture switch (\(-\text{AJF}\)) for all CTOOLS that require you to specify an architecture. (You can also set the \$I960ARCH\ or \$G960ARCH\ environment variables to \text{JF}.) You can still simplify future migration efforts by staying within the boundaries of the \(-\text{ARP}\) switch whenever possible. See Details of the Rx Strategy for information on the requirements.

For low-level processor functionality such as disabling interrupts, cache control, or atomic accesses you may wish to use the new assembler pseudo-instructions detailed in Improved Pseudo-instruction Support for \text{gas960/asm960}. This, too, may ease future migration without excluding use of JF-specific constructs.

Details of the Rx Strategy

80960 Instruction Set Support

The implementation of the \(-\text{ARx}\) architecture options have been redefined in CTOOLS to represent a subset of the i960 Jx processor instruction set chosen for performance and future compatibility reasons. These restrictions are enforced by the assembler and other tools when an \(-\text{ARx}\) switch is used or when an i960 Rx architecture is specified using the \text{I960ARCH}\ or \text{G960ARCH}\ environment variables.
The following i960 Jx processor instructions are not supported with the i960 Rx architectures:

- addi
- addi<cc>
- atadd
- atmod
- cmpdeci
- cmpdeco
- cmpinci
- cmpinco
- comcmpi
- comcmpo
- eshro
- extract
- fault<cc>
- halt
- intctl
- ldt
- mark
- modac
- modi
- modify
- modtc
- movl
- movq
- movt
- notor
- xnor
- remo
- shli
- shrdi
- spanbit
- stib
- stis
- stt
- subi
- subi<cc>
- syslogL
- test<cc>

In addition, the following addressing mode restrictions exist for MEM format instructions when specifying an i960 Rx processor-based target:

- Indexed addressing modes are not available.
- IP-relative addressing is not available.
- Two-word MEM-format is not available for the following instructions:
  - ldl
  - std
  - ldq
  - std
  - bx
  - callx
- The balx instruction may only use register-indirect addressing (no offsets or displacements allowed).
Other consequences of using the 80960Rx output architectures are:

- The `calls` instruction may use register g13 or a literal as its target only.
- For the `modpc` instruction, the mask cannot specify the same register as the src/dst register.
- The Process Controls register is undefined in the Rx architecture, so use of the `modpc` instruction is not recommended.
- The `scanbit` instruction is not guaranteed to set the condition code. The following instruction sequence duplicates the functionality of the `scanbit` instruction and is guaranteed to set the condition code:
  ```assembly
  scanbit    src1,dst
  notbit    31,dst,dst
  chkbit    31,dst,dst
  notbit    31,dst,dst
  ```
- The `calljx` pseudo-instruction requires a second argument, a temporary register into which the address of the first argument can be loaded.
- The assembler recognizes `call4`, `call8`, and `call12` instructions. These instructions are identical to the traditional `call` instruction except that the two low-order (reserved) bits of the instruction word are set as shown:

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>call4</code></td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td><code>call8</code></td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td><code>call12</code></td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

- The assembler recognizes `call4j`, `call8j`, and `call12j` pseudo-instructions. They are treated by the assembler identically to the `callj` pseudo-op except they set the low-order bits as indicated in the table above if they are optimized into corresponding `call4`, `call8`, or `call12` instructions.
In addition, a new assembler pseudo-op has been added:

```
b_960a  label
```

This pseudo-op is reserved and should not be used by application software. The assembler generates an instruction, a no-op instruction, whose execution effectively leaves the state of the existing 80960Rx, 80960Jx, and 80960Hx processors unchanged. It is uncertain if this pseudo-op will continue to function in the same manner on future 80960 processors.

The assembler will generate the following no-op instruction for a `b_960a label` pseudo-op:

```
addino TARG,fp,fp
```

where TARG is (label-IP-4)/4 and 0 ≤ TARG ≤ 15

**Big-Endian Support**

Big endian byte order is not supported when code is being generated for the i960 Rx processors.

**b.out OMF Support**

gas960, the b.out assembler, does not support an i960 Rx target.
80960 Assembly Language Converter (xlate960)

To ease the task of converting legacy assembly language code for use with the new i960 Rp/Rd processors, CTOOLS 6.0 includes xlate960. The xlate960 program converts assembly language code from 80960 core processors (e.g., i960 Cx, Jx, and Hx processors) to its CORE0 (e.g., 80960Rx) equivalent. xlate960 performs both instruction translations and addressing-mode translations. Instruction translation occurs when the target architecture does not support a translatable instruction from the source architecture (e.g., movt). Addressing mode translation occurs when the target architecture supports a restricted form of an instruction from the source architecture (e.g., callx). For more information on xlate960, see the i960 Processor Software Utilities Manual.

Improved Assembler Pseudo-instruction Support

Introduction

A number of pseudo-instructions have been added to the CTOOLS assembler to ease migration between processors. These pseudo-ops provide an architecture-independent method for performing some of the more common low-level processing operations. Using these pseudo-ops should reduce the number of changes required when moving assembly code from one i960 processor to another. Table 2-1 lists all of the new pseudo-instructions supported by the CTOOLS assembler. See Chapter 8 for descriptions of the new pseudo-ops and instructions on using them.
Table 2-1 New Assembler Pseudo-Ops

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>atomic_add</td>
<td>Atomic add</td>
</tr>
<tr>
<td>atomic_modify</td>
<td>Atomic modify</td>
</tr>
<tr>
<td>bkpt_request</td>
<td>Request breakpoint resources</td>
</tr>
<tr>
<td>cc_read</td>
<td>Read condition code</td>
</tr>
<tr>
<td>cc_scanbit</td>
<td>Scan for bit, modifying condition code</td>
</tr>
<tr>
<td>dc_disable</td>
<td>Disable data cache</td>
</tr>
<tr>
<td>dc_enable</td>
<td>Enable data cache</td>
</tr>
<tr>
<td>dc_invalidate</td>
<td>Invalidate data cache</td>
</tr>
<tr>
<td>em_read</td>
<td>Read execution mode</td>
</tr>
<tr>
<td>ic_disable</td>
<td>Disable instruction cache</td>
</tr>
<tr>
<td>ic_enable</td>
<td>Enable instruction cache</td>
</tr>
<tr>
<td>ic_invalidate</td>
<td>Invalidate instruction cache</td>
</tr>
<tr>
<td>ic_load_lock</td>
<td>Load and lock instruction cache</td>
</tr>
<tr>
<td>insn_trace_mode_read</td>
<td>Read instruction trace mode</td>
</tr>
<tr>
<td>insn_trace_mode_set</td>
<td>Set instruction trace mode</td>
</tr>
<tr>
<td>interrupt_state</td>
<td>Read interrupt state</td>
</tr>
<tr>
<td>ip_read</td>
<td>Read instruction pointer</td>
</tr>
<tr>
<td>pri_read</td>
<td>Read execution priority</td>
</tr>
<tr>
<td>sw_reinit</td>
<td>Reinitialize processor</td>
</tr>
<tr>
<td>trace_enable_set</td>
<td>Set trace enable bit</td>
</tr>
</tbody>
</table>
This chapter discusses the assembler invocation syntax, options, input, and output and explains how to automate assembly. You can invoke the assembler from the operating system prompt or from a script or batch file.

**Invocation Command**

Invoke the assembler as follows:

```
asm960 | gas960 [ c | e ] [-option]... [source]... [...]
```

- `asm960` or `gas960c` invokes the assembler to generate COFF output. The dual syntax provides backwards compatibility with previous versions of the iC-960 and gcc960 C compilers.
- `gas960` invokes the assembler to generate b.out format output.
- `gas960e` invokes the assembler to generate ELF format output.
- `option` is an invocation option (described in Chapter 4) affecting assembler input, operation, and output. Arguments can follow some options. Case is significant.
- Precede the options with a hyphen (-). In Windows, you can use a slash (/) instead of the hyphen.
- `source` is an assembly source filename. You can provide a complete path name for each source file. The default search path is the current directory.
You can interleave options and source filenames.

**NOTES.** On UNIX, case is significant for all parts of the assembler invocation syntax. In Windows, case is significant only for the options and option arguments.

*Examples throughout this manual use a UNIX host system and the gas960e invocation command and directory structures, unless otherwise noted.*

*The b.out assembler does not support the i960 RD/RP Processors.*

### Specifying Option Arguments

Some options require arguments. The assembler interprets any string following such an option as the option argument. Omitting an option argument at the end of the command line causes an error. For example:

```
    gas960e myprog.as -o
    gas960: Expected a filename after -o.
```

You can put a space between an option and its argument. The following are both correct:

```
    gas960e myprog.as -omyprog.o
    gas960e myprog.as -o myprog.o
```

An incorrect argument causes an error message appropriate to the option. See Chapter 4, Option Reference, for information on the valid arguments for each option.

### Specifying Single and Multiple Options

Precede options with a hyphen (-):

```
    gas960e myprog.as -o myprog.obj -W -V
```
On Windows® 95/Windows NT*-based machines, you can use a slash (/) instead of the hyphen.

Any string that does not begin with a hyphen and is not positioned as an option argument is interpreted as a source filename. The following example shows the message caused when the V option is specified without a hyphen and no file named V is in the search path:

```
gas960e -W V myprog.as
Can't open V for reading.
No such file or directory.
```

Some options consist of a single character with no arguments. You can specify two or more such options as an option group with a single hyphen:

```
gas960e myprog.as -o myprog.obj -WV
```

Using Uppercase and Lowercase

Depending on your host system, case can be significant in the assembler invocation name. For example, on Windows, entering ASM960 is the same as entering asm960. On UNIX, you can invoke the assembler with asm960 but not with ASM960.

Regardless of your host system, case is significant in the options and arguments. For example, an uppercase W is valid, but a lowercase w causes the following message:

```
Unrecognized option: w
```
Naming the Object File

After a successful assembly, the assembler produces an object file in common object file format (COFF), b.out or ELF format. To generate a COFF object file, invoke the assembler with *asm*960 or *gas*960c. To generate a b.out format object file, invoke the assembler with *gas*960. To generate an ELF file, use *gas*960e. For a description of the COFF file format, see your utilities user’s guide. For a description of ELF, see the Intel 80960 EABI specification (Intel Literature order number 631999) listed in *Getting Started*.

When you specify a source file with the .s or .as extension, the assembler creates an object file with the extension .o. When you specify a file with any other extension (or none) the assembler creates an object file with full source filename (including its original extension) with .o appended.

When you provide the first block of input interactively, the object filename is a.out for COFF output, b.out for b.out format output, and e.out for ELF output. For example, the following produces a single object file named ex1.o:

```
gas960e ex1.s ex2.s ex3.s
```

To specify the object filename, use the o option. For example, the following creates or replaces an object file named ex1.o:

```
gas960e example.src -o ex1.o
```

The assembler can overwrite an existing file unless the filename ends in .s, .as, or .asm. To ensure your source files are not accidentally overwritten, use the protected filename extensions. For example, if ex1.s exists, the following stops assembly with an error:

```
gas960e example.s -o ex1.s
```

```
FATAL: Output file will overwrite existing protected file.
```

Additional software utilities are available to read and reformat the object file, as described in the *i960 Processor Software Utilities User’s Guide*. 
Providing Source Input

You must provide source text from at least one of:
- a file named in the assembler invocation command
- stdin, such as the keyboard or the redirected output of another command

For information on stdin, see your host operating system documentation.

An assembly source file is an ASCII file of assembly language instructions and assembler directives. You can write the assembly source using a text editor or generate an assembly file with the C compiler.

For interactive input, specify the i option and provide lines of assembly source from stdin (for example, lines entered from the keyboard or piped from another application). The following example pipes the output of a script named mybuild (invoked with the UNIX C shell primitive source command) into the assembler:

```
source mybuild | gas960e -i
```

For information on piping, see your host operating system documentation.

To end keyboard input, type the Ctrl-d key combination on a new line.

The following keyboard-entry example assembles five lines, naming the output object file e.out:

```
gas960e -i
roundr g0, fp0
subr fp0, g0, g0
expr g0, g0
addr 1.0, g0, g0
scaler g1, g0, g0
^d
```

In the invocation command, list sources in the order in which you want them assembled. The assembler concatenates all source files and interactive input, then assembles instructions and data into sections by order of appearance in the source text.
The following example assembles source from `ex1.s`, then from interactive input (the `i` option), then from `ex2.s`. Program elements from any one block of the input (for example, `ex1.s`) are available to any other block of the input (for example, `ex2.s`) as if all the input were in a single, sequential file.

```
gas960e ex1.s -i ex2.s
```

You can use other assembler options and source files with interactive input. The following example displays the assembler version and begins interactive input from the keyboard:

```
asm960 -V -i
```

To ensure your source files are not accidentally overwritten, use the `.s`, `.as`, or `.asm` protected filename extensions, as described in Naming the Object File on page 3-4.

### Environment Variables

Environment variables set default operating parameters, such as search paths and the target architecture. For a list of environment variables and their uses, see your *Getting Started* manual. Define the environment variables before invoking the assembler.

The assembler supports all I960 and G960 environment variables, preferring those that match the invocation style. For example, when you invoke the assembler as `asm960`, the assembler looks first for I960 environment variables, and for those settings not found, looks for G960 environment variables. The environment variables used by the assembler are listed in Table 3-1.
Table 3-1  Assembler Environment Variables

<table>
<thead>
<tr>
<th>gnu Tools Name</th>
<th>CTOOLS Name</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>G960ARCH</td>
<td>I960ARCH</td>
<td>Specifies target architecture.</td>
</tr>
<tr>
<td>G960IDENT</td>
<td>I960IDENT</td>
<td>Allows use of the COFF .ident directive.</td>
</tr>
<tr>
<td>G960INC</td>
<td>I960INC</td>
<td>Specifies include directory path.</td>
</tr>
<tr>
<td>G960BASE</td>
<td>I960BASE</td>
<td>Specifies base environment directory.</td>
</tr>
<tr>
<td>G960XLT</td>
<td>I960XLT</td>
<td>Specifies translator (xlate960) location.</td>
</tr>
</tbody>
</table>

For more information on environment variables, see your host operating system documentation.

Selecting the Instruction Set and Libraries

The assembler reports an error for any instruction in your source text that is not valid for your target processor instruction set. To assemble for a specific i960 processor, you can define the I960ARCH or G960ARCH architecture environment variable. Then, you need use the A option (described in Chapter 4) only to override the environment variable. Leaving the environment variable undefined and omitting the A option assembles for the i960 KB architecture.

To specify the default instruction set, define the architecture environment variable as SA, SB, KA, KB, CA, CF, JA, JD, JF, JT, RD, RP, HA, HD or HT. For example, the following specify SA instructions unless a different processor is specified with the A option:

```
csh     setenv I960ARCH SA
sh or ksh  I960ARCH=SA; export I960ARCH
```

Other i960 processor software tools also use the architecture environment variable, as described in Getting Started.
Defining a Base Directory Path

You can set an environment variable to the assembler and utilities base directory. Such a value can be useful for setting other search-path environment variables. The following defines a base-directory environment variable named G960BASE:

```
csh       setenv G960BASE /usr/local/intel960
sh or ksh  G960BASE=/usr/local/intel960;export G960BASE
```

Defining an Identification String

To put assembler identification and information from the .ident directive into a COFF object file, define the I960IDENT or G960IDENT environment variable to any non-null value, as shown in the following example:

```
csh       setenv I960IDENT 1
sh or ksh  I960IDENT=1;export I960IDENT
```

Redirecting Error and Warning Message Output

The I960ERR variable lets you specify whether messages are directed to stdout or stderr. When I960ERR is not set, messages go to stdout. When I960ERR is set to a non-null string, the output goes to stderr. This variable functions under Windows only.

Building a Search Path for Include Files

You can extend the search path as follows for files included with .include:

- The assembler always searches the current directory first.
- You can specify additional directories with the I option, described in Chapter 4, Option Reference.
- You can specify a default list of directories, separated with colons (:), with I960INC or G960INC. When you do not use the I option, the assembler searches the directories specified by I960INC or G960INC.
Note that when you use both the I option and the I960INC or G960INC variables, the environment variable setting takes precedence.

The following commands set G960INC to
/usr/local/intel960/include:

```
csh   setenv G960INC /usr/local/intel960/include
sh or ksh G960INC=/usr/local/intel960/include;export G960INC
```

**Building the Search Path for the Assembler Executable**

To invoke the assembler from any directory, add the assembler directory to your PATH environment variable. Once the directory is in your PATH, you need not use the directory path name to invoke the assembler.

For example, with I960BASE set to your assembler base directory, you can augment your PATH as follows:

```
csh   setenv PATH $I960BASE/bin:$PATH
sh or ksh PATH=$I960BASE/bin:$PATH;export PATH
```
This chapter describes the assembler options alphabetically. Table 4-1 summarizes the option names, arguments, effects, and defaults.

The following notation is used in this chapter:

\{item \mid item\} Select one of the items listed between braces. A vertical bar (|) separates the items.

\[items\] Items enclosed in brackets are optional.

### Table 4-1 Assembler Options

<table>
<thead>
<tr>
<th>Option</th>
<th>Effect of the Option</th>
<th>Default Action of the Assembler</th>
</tr>
</thead>
<tbody>
<tr>
<td>A { SA</td>
<td>SB</td>
<td>KA</td>
</tr>
<tr>
<td>D sym[=value]</td>
<td>defines an absolute symbol. Symbols defined in this way can be used in .if and .ifdef expressions.</td>
<td>symbols must be defined in the source text.</td>
</tr>
<tr>
<td>d</td>
<td>retains debug information for local symbols beginning with L or a dot (.).</td>
<td>discards symbolic information for local symbols beginning with L or a dot (.).</td>
</tr>
<tr>
<td>G</td>
<td>generates big-endian COFF or ELF code.</td>
<td>generates little-endian code.</td>
</tr>
</tbody>
</table>

continued ☛
## Table 4-1 Assembler Options (continued)

<table>
<thead>
<tr>
<th>Option</th>
<th>Effect of the Option</th>
<th>Default Action of the Assembler</th>
</tr>
</thead>
<tbody>
<tr>
<td>h</td>
<td>Help: prints a brief description of each option.</td>
<td>no help text is printed.</td>
</tr>
<tr>
<td>I directory path</td>
<td>adds directories to the search path for include files.</td>
<td>searches in the current directory and uses the I960INC or G960INC environment variable.</td>
</tr>
<tr>
<td>i</td>
<td>reads source from stdin.</td>
<td>reads source from files.</td>
</tr>
<tr>
<td>L list_options</td>
<td>generates a listing. Listing sub-options modify the listing behavior.</td>
<td>no listing is generated.</td>
</tr>
<tr>
<td>n</td>
<td>do not replace compare-and-branch instructions.</td>
<td>replaces compare-and-branch instructions.</td>
</tr>
<tr>
<td>o objfile</td>
<td>specifies an object filename.</td>
<td>uses a.out, b.out, e.out, or a filename derived from the first source filename.</td>
</tr>
<tr>
<td>p (c</td>
<td>d</td>
<td>b)</td>
</tr>
<tr>
<td>V</td>
<td>displays a version message and continues the assembly.</td>
<td>displays no version message.</td>
</tr>
<tr>
<td>v960</td>
<td>displays a version message and stops the assembly.</td>
<td>displays no version message; the assembly proceeds.</td>
</tr>
<tr>
<td>W</td>
<td>suppresses the warning messages.</td>
<td>displays the warning messages.</td>
</tr>
<tr>
<td>x</td>
<td>generates warnings about architecture mismatches.</td>
<td>generates error message when it encounters architecture mismatch.</td>
</tr>
<tr>
<td>z</td>
<td>suppresses the object file header time-and-date stamp for COFF assembler.</td>
<td>writes the assembly time and date in the object file header.</td>
</tr>
</tbody>
</table>
A: Architecture

Select the architecture
(instruction set)

A arch

arch

is SA, SB, KA, KB, CA, CF, JA, JD, JF, JT, RD, RP, HA, HD, HT, CORE0, CORE1, CORE2, CORE3, or ANY.

Discussion

To select your i960 processor instruction set, specify the A option. The assembler displays an error message for each instruction in the source text that is invalid for the selected architecture, or a warning when you use the X option.

Without the A option, the assembler uses the instruction set specified by the I960ARCH or G960ARCH environment variable. If the architecture environment variable is undefined, the assembler uses the KB instruction set.

New CORE Architecture Options

With CTOOLS release 5.1 and later, the assembler supports architecture settings to allow the generation of code that is compatible with multiple i960 processor types. These settings are referred to as core architectures. Table 4-2 shows the types of i960 processors that are supported by each core architecture.
Table 4-2  CORE0-3 Architecture Compatibilities

<table>
<thead>
<tr>
<th>-A Switch Used</th>
<th>Compatible Architectures</th>
</tr>
</thead>
<tbody>
<tr>
<td>CORE0</td>
<td>Jx, Hx, Rx</td>
</tr>
<tr>
<td>CORE1</td>
<td>Kx, Sx, Cx, Jx, Hx</td>
</tr>
<tr>
<td>CORE2</td>
<td>Jx, Hx</td>
</tr>
<tr>
<td>CORE3</td>
<td>Cx, Jx, Hx</td>
</tr>
</tbody>
</table>

D: Define symbol

Define an absolute symbol from the command line

D symbol [=value]

symbol is the name of the symbol you want to create.

value is any valid non-relocatable expression.

Discussion

This option is intended to be used with the .if and .ifdef directives for conditional assembly. It resembles the similar compiler preprocessor option. If =value is left blank, then the value of name is set to 1. If you want to include spaces anywhere with symbol=value, then the entire symbol=value must be quoted.
Examples

The following creates a symbol called foo and sets its value to 1:

```
gas960 -D foo file.s
```

Within file.s, both of the following would evaluate to true:

```
.if foo
.ifdef foo
```

```
gas960 -D "foo = bar * 12" file.s
```

Within file.s, the symbol bar must be defined and be non-relocatable.

```
gas960 -D foo=0 file.s
```

Within file.s, the expression

```
.ifdef foo
```

is true, but the expression

```
.if foo
```

is false. (See the discussion of .if and .ifdef in Chapter 5.)
d: Debug symbols

Keep debugging information about assembler temporary symbols

d

Discussion

The assembly output from the compiler contains local symbols beginning with an L, as generated by a gcc960 invocation of the compiler, or a dot (.), as generated by an ic960 invocation of the compiler. To retain such symbols in the object-file symbol table, specify the d option. Without d, the assembler removes all such local symbols.

Examples

The following shows the original C source text and the corresponding assembly output with the local symbols generated by a gcc960 invocation of the compiler:

```c
if (a==b)
    hi=b;
else
    hi=c;
```

The compiler assembly output (in the file cmset.s) is:

```assembly
cmpi  g0,g1
be    L1
b     L2
L1:  st  g1,hi
    b   A1
L2:  st  r6,hi
A1:  
```

The following puts L1 and L2 in the object-file symbol table:

`gas960c -d cmset.s`
G: Big-endian target

*Produce a COFF or ELF file for a big-endian target*

**Discussion**

You can configure COFF or ELF program text-type and data-type sections in either big-endian or little-endian byte order. For big-endian instructions and data, specify the `G` option when:

- assembling for the C-series, J-series, or H-series architecture
- invoking the assembler with `asm960` or `gas960c` (COFF only) or `gas960e` (ELF only)

Note that the i960 RD/RP processors do not support big-endian byte order, even though their core processor is an 80960Jx.

For byte-order information, see *C: A Reference Manual*.

**Example**

The following produces a COFF file for a big-endian target. The .text- and .data-style sections of the COFF file is in the host byte order, regardless of the `G` option.

```
gas960c -G -ACA big.a
```
I: Include-file search path

Augment the search path for include files

I path

path is a directory pathname.

Discussion

The assembler always searches the current directory for .include filenames. You can augment the search path by:

• defining the I960INC or G960INC environment variable (described in Chapter 3) before invoking the assembler
• using the I option once or more when invoking the assembler

The search path sequence is:
1. the current working directory
2. any directories specified by I960INC or G960INC, in the order defined
3. any directories specified with I, in the order on the command line

Example

The following line in the mathr.s source file includes the /mylib/fp.s source file:

.include "fp.s"

when invoked as:

asm960 mathr.s -I/mylib
i: Input from stdin

Include keyboard or redirected input

Discussion

You must provide source text from at least one of:

- a filename specified on the command line
- the keyboard, the redirected output of another command, or any other device designated as stdin

For stdin input, use the i option once in the assembler invocation. To assemble keyboard input, after entering the command line, enter lines of source text from the keyboard. To end the keyboard input, enter the Ctrl-d key sequence on a new line. To assemble redirected output from another application, pipe the application output into the assembler invocation. You need not enter Ctrl-d to end the redirected input.

You can use both the i option and zero or more source filenames. The assembler processes the stdin input in sequence with any source files.

When stdin is the first or only source specified on the command line, the default object filename is a.out for a COFF object file, b.out for a b.out-format object file, and e.out for an ELF format object file. Use the o option to specify a different object filename.

For information on piping and on stdin, see your host system manual.
Examples

1. The following assembles several lines of code from the keyboard after the source text from the predef.s file:
   ```
gas960e predef.s -i
   roundr g0, fp0
   subr fp0, g0, g0
   expr g0, g0
   addr 1.0, g0, g0
   scaler g1, g0, g0
   ^d
   ```

2. The following assembles the output from the getpatch script (invoked with the csh primitive source command) between src1.s and src2.s:
   ```
   source getpatch | gas960e src1.s -i src2.s
   ```

L: Generate a listing

*Print an assembly listing on the screen or into a file*

```
L [option [option-arg]]
```

- option is one of the following:
  - a: list all lines, ignoring .nolist directives.
  - e: list text and data in target-endian byte order.
  - f: print the listing into a file. option-arg is the name of the file.
  - n: do not list files included with .include.
  - t: use option-arg as the listing title. If the title contains spaces, then it must be quoted. This option overrides .title directives in the source.
  - z: do not print the listing header.
Option Reference

Discussion

With no options, the listing is printed on the standard output and all listing defaults are in effect. Options that do not take arguments can be catenated together (with no spaces) after a single \( L \) option. Space is optional between an option that takes an argument and the argument.

The byte order of the listing is always target-endian when listing data sections. For text sections, instructions are printed big-endian ("left-to-right") unless you specify \( Le \), and then they are printed in target-endian byte order.

Examples

Several example listings follow. Where appropriate, the contents of the assembly language file is also shown. The first example shows the simplest listing invocation.

The file listex1.s contains:

```assembly
.title "Listing Example 1"
.text
  mov g0,g1
.data
  .short 0x1234
```

The assembler invocation command is:

```
$ gas960e -L listex1.s
```
Listing Example 1
Number of errors: 0
Number of warnings: 0
Source File: listex1.s
1 000000 .title "Listing Example 1"
2 000000 .text
3 000000 5c881610 mov g0,g1
4 000004 .data
5 000004 3412 .short 0x1234

The next example shows -Lz, (don't print the listing header), and -Lf, (print listing in a file).
$ gas960 -Lz -Lf listex1.L listex1.s
The file listex1.L contains:
Source File: listex1.s
1 000000 .title "Listing Example 1"
2 000000 .text
3 000000 5c881610 mov g0,g1
4 000004 .data
5 000004 3412 .short 0x1234

The next example shows the effect of the .nolist directive on the listing.
The file listex2.s contains:
.title "Listing Example 2"
.text
mov g0,g1
.data
.short 0x1234
.nolist
.asciz "Skip strings in the listing"
.asciz "Skip this one too"
.list
.word 0x12345678
Option Reference

The assembler command is:

```
$ gas960e -L listex2.s
```

Listing Example 2
Number of errors: 0
Number of warnings: 0
Source File: listex2.s

```
1 000000                      .title     "Listing Example 2"
2 000000                      .text
3 000000 5c881610              mov     g0,g1
4 000004                      .data
5 000004 3412                  .short     0x1234
6 000006                      .nolist
7 000006                      .list
8 000006 7856 3412            .word     0x12345678
```

The .nolist directive can be defeated from the command line with -La:

```
$ gas960c -Lza listex2.s
```

Source File: listex2.s

```
1 000000                      .title     "Listing Example 2"
2 000000                      .text
3 000000 5c881610              mov     g0,g1
4 000004                      .data
5 000004 3412                  .short     0x1234
6 000006                      .nolist
7 000006 536b 69702073         .asciz "Skip strings in the listing"
8 000006 7472696e 6773206f746f7020746865206c697374696e6700
9 000022 536b 697020746865206c697374696e6700
10 000024 6e6973206f6e6520746f6f00
11 000034                      .list
12 000034 78563412            .word     0x12345678
```
Normally, text sections are listed in big-endian byte order. This matches left-to-right ordering of instructions in manuals. You can override this behavior on the command line with \-le. Note in the next example that the listing show the exact ordering of bytes in the object file:

```
$ gas960c -Lze listex2.s
```

Source File: listex2.s
1 000000                   .title "Listing Example 2"
2 000000                   .text
3 000000 1016885c           mov g0,g1
4 000004                   .data
5 000004 3412               .short 0x1234
6 000006                   .nolist
9 000034                   .list
10 000034 78563412           .word 0x12345678

Here is another example that shows big-endian byte order in both the text and data sections:

```
$ gas960c -ACA -G -Lze listex2.s
```

Source File: listex2.s
1 000000                     .title "Listing Example 2"
2 000000                     .text
3 000000 5c881610           mov g0,g1
4 000004                     .data
5 000004 1234               .short 0x1234
6 000006                     .nolist
9 000034                     .list
10 000034 12345678           .word 0x12345678

The next example shows the effect of the .include directive on the listing. The file listex3.s contains:

```
.title "Listing Example 3"
.text
  mov g0,g1
.include "listex4.s"
```

Source File: listex3.s
1 000000                   .title "Listing Example 3"
2 000000                   .text
3 000000 1016885c           mov g0,g1
4 000004                   .data
5 000004 3412               .short 0x1234
6 000006                   .nolist
9 000034                   .list
10 000034 78563412           .word 0x12345678

The next example shows the effect of the .include directive on the listing. The file listex3.s contains:

```
.title "Listing Example 3"
.text
  mov g0,g1
.include "listex4.s"
```

Source File: listex3.s
1 000000                   .title "Listing Example 3"
2 000000                   .text
3 000000 1016885c           mov g0,g1
4 000004                   .data
5 000004 3412               .short 0x1234
6 000006                   .nolist
9 000034                   .list
10 000034 78563412           .word 0x12345678

```
```
The file listex4.s contains:

```
foo:
  ldconst -1, g6
```

The assembler command is:

```
$ gas960 -Lz -D INCLUDE4 listex3.s
```

Source File: listex3.s
1  000000                     .title "Listing Example 3"
2  000000                     .text
3  000000  5c881610           mov g0,g1
4  000004                     .ifdef INCLUDE4
5  000004                     .include "listex4.s"
6  000008                     .endif
7  000008                     .data
8  000008  3412               .short 0x1234

Source File: ./listex4.s
1  000004                     foo:
2  000004  59b01901           ldconst -1, g6

Source File: listex3.s
6  000008                     .endif
7  000008                     .data
8  000008  3412               .short 0x1234

You can tell the assembler to not list include files with -Ln:

```
$ gas960 -Lzn -D INCLUDE4 listex3.s
```

Source File: listex3.s
1  000000                     .title "Listing Example 3"
2  000000                     .text
3  000000  5c881610           mov g0,g1
4  000004                     .ifdef INCLUDE4
5  000004                     .include "listex4.s"
6  000004                     .endif
7  000004                     .data
8  000008  3412               .short 0x1234

The last example shows how to override the .title directive from the command line with -Lt:

```
$ gas960e -Lt "LISTING EXAMPLE 247" listex3.s
```

You can tell the assembler to not list include files with -Ln:
n: No compare-and-branch replacement

Do not replace compare-and-branch instructions

Discussion

For short conditional branches and jumps, you can save execution time and space by using a single compare-and-branch (COBR) instruction. The branch address can be any expression that evaluates to a 13-bit value.

To stop the assembler with an error when the branch address is out of range, specify the $n$ option. Without $n$, the assembler replaces the short-range compare-and-branch instruction with two instructions.
Examples

1. In the following, \( n \) prevents the assembler from expanding the `cmpibe` instruction for the undefined external \( m1 \). The assembler displays an error message.

   $\ text{gas960e -i -n}$
   `cmpibe g0.gl.ml`
   `\^D`
   `can't use COBR format with external label`

2. Without \( n \), and with the \( s \) option, the following replaces `cmpibe`:

   | 0: | 5a046090 | cmpi g0.gl |
   | 4: | 12fffffc | be m1      |

---

**o: Object filename**

*Name the object file*

\( o \) \( objfile \)

\( objfile \) is a valid filename.

**Discussion**

To specify the object filename, use the \( o \) option with a filename or a complete pathname. The default object filename is in the current directory:

- a filename based on the first source filename on the command line, replacing any `.s` or `.as` source-filename extension with `.o` or appending `.o` to any other source filename after the extension.
- `a.out`, when you invoke the assembler with `asm960` or `gas960c` (for COFF output) with interactive input as the first or only source.
- `b.out`, when you invoke the assembler with `gas960` (for `b.out-format` output) with interactive input as the first or only source.
- `e.out`, when you invoke the assembler with `gas960e` (for ELF output) with interactive input as the first or only source.
To avoid accidentally overwriting your source files, use a protected `.s`, `.as`, or `.asm` source-filename extension (the assembler does not overwrite existing files with one of these extensions).

Example

The following names the output file `prog1.o`:

```
asm960 myprog.asm -o prog1.o
```

p: Position independence

Mark the COFF or ELF object file as containing position-independent code or data

```
p type
```

<table>
<thead>
<tr>
<th>type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>c</td>
<td>indicates position-independent code.</td>
</tr>
<tr>
<td>d</td>
<td>indicates position-independent data.</td>
</tr>
<tr>
<td>b</td>
<td>indicates both position-independent code and data.</td>
</tr>
</tbody>
</table>

Discussion

To indicate position-independent code or data in the COFF or ELF file, use the `p` option. You can also use the `.pic`, `.pid`, and `.link_pix` directives, described in Chapter 5.

Example

The following marks the object file as position-independent:

```
asm960 -pb mypi23.s
```
t: Translate

Process all source files with the xlate960 translation utility before assembly

Discussion

To first process the input source file with xlate960, use t. xlate960 attempts to translate the source file to its CORE0 (e.g., 80960Rx) equivalent. If any errors occur during the translation process, the assembler does not attempt to process the xlate960 output file. This includes instances where the translator output file requires manual adjustments.

Example

The following shows an example invocation of xlate960 from the assembler command-line:

$ cat myprog.s
addino r5,r6,r7
$ gas960e myprog.s -t -ARP
$ gdmp960 myprog.o

Section `.text`:

0: 78398005 addono r5,r6,r7

Section `.data`:

In this example, the translator converted the 80960 CORE instruction addino with the 80960 CORE0-compatible instruction addono.
NOTE. The t (translate with xlate960) option is incompatible with the i (process input from stdin) command-line option.

V, v960: Version
Display the assembler version number and creation date

\{V \ v960\}

Discussion
To display a version message on stdout during assembly, use V. After displaying the message, the assembler continues. For information on stdout, see your host system manual.

To display the message without assembling, use v960. After displaying the message, the assembler stops.

The message includes the assembler version number and the assembler creation date and time.

Example
The following shows a sample version message:

$ gas960e myprog.asm -v960

Intel 80960 ELF Assembler, 6.0.6002, Thu Sep 26 23:25:43 MST 1997
W: Warnings

*Suppress the warning messages*

To suppress the warning messages, use `W`. The error messages continue to appear on `stderr`. For information about the message formats, see Chapter 6. For information on `stderr`, see your host system manual.

x: Allow mixed architectures

*Allow architecture mismatches*

Using the `x` option causes the assembler to generate warnings (not errors) when it encounters mixed architectures (e.g., opcode not in target architecture).
Example

The following shows how using the x command-line switch affects the assembler’s treatment of architecture-specific instruction mismatches:

```bash
$ cat myprog.s
xnor  r5,r6,r8
stl   r8,r10(g10)[g4*4]
$ gas960e myprog.s -ARP
myprog.s:1: Opcode is not in target architecture: "xnor".
myprog.s:2: indexed addressing mode not available
$ ls myprog.o
ls: myprog.o: No such file or directory
$ gas960e myprog.s -ARP -x
myprog.s:1: Warning: Opcode is not in target architecture: "xnor".
myprog.s:2: Warning: indexed addressing mode not available
$ ls myprog.o
myprog.o
```

$
z: Time stamp

Suppress the time stamp in the COFF output file

Discussion

The assembler puts the current time and date in the file header of the COFF output file. On most UNIX systems, to put Time Zero in place of the current time stamp, specify z. Time Zero is 4:00, 31 December, 1969.

The z option has no effect on b.out or ELF format output.

Example

The following command specifies Time Zero for the time stamp:

gas960e -z file1.s
Directives

This chapter describes how to use the assembler directives in your source text. The Directives Reference section, which begins on page 5-10, provides an encyclopedia of the directives.

Table 5-1 Functions Performed by Directives

<table>
<thead>
<tr>
<th>Category</th>
<th>Function</th>
<th>Directives</th>
</tr>
</thead>
<tbody>
<tr>
<td>input-specification</td>
<td>specify how the assembler finds and reads input and controls conditional assembly.</td>
<td>.if, .else, .endif, .ifdef, .ifndef, .ifnotdef, .include</td>
</tr>
<tr>
<td>location-counter control</td>
<td>change the location counter and specify program sectioning.</td>
<td>.align, .bss, .data, .org, .section, .text</td>
</tr>
<tr>
<td>data and memory initialization</td>
<td>assemble data in integer, ordinal, and real formats and initialize strings and memory blocks.</td>
<td>.ascii, .asciz, .byte, .double, .extended, .fill, .float, .single, .int, .long, .word, .short, .hword, .space</td>
</tr>
<tr>
<td>symbol and debugger- support</td>
<td>define symbols and provide source and symbolic information for debugging.</td>
<td>.comm, .def, .ifdef, .desc, .elf_size, .elf_type, .equ, .global, .globi, .set, .lsym, .file, .lcomm, .line, .ln, .stabd, .stahn, .stabs, .scl, .size, .tag, .type, .val</td>
</tr>
<tr>
<td>optimization</td>
<td>optimize memory addressing and procedure calls.</td>
<td>.leafproc, .jomem, .sysproc</td>
</tr>
</tbody>
</table>

continued ➝
Table 5-1  Functions Performed by Directives (continued)

<table>
<thead>
<tr>
<th>Category</th>
<th>Function</th>
<th>Directives</th>
</tr>
</thead>
<tbody>
<tr>
<td>identification</td>
<td>identifies the assembly.</td>
<td>.ident</td>
</tr>
<tr>
<td>abort</td>
<td>stops the assembly.</td>
<td>.ABORT</td>
</tr>
<tr>
<td>position-independence</td>
<td>mark object files as position-independent.</td>
<td>.pic, .pid, .link_pix</td>
</tr>
<tr>
<td>listing</td>
<td>control listing behavior.</td>
<td>.list, .nolist, .title, .eject</td>
</tr>
</tbody>
</table>

NOTE. To assemble directives relevant for COFF development, invoke the assembler as asm960 or gas960c. For directives relevant for b.out-format development, use gas960. For directives relevant to ELF development, use gas960e.

Syntax

For the directives in your source text, use the following syntax:

```
.name arg_string
```

`name` is the directive keyword. The leading dot (.) is required.

`arg_string` is zero or more arguments, according to the requirements of the directive.
Specifying the Input

When invoking the assembler, you must specify a source file on the command line, as described in Chapter 3. For additional source text, you can include the contents of other files with the .include directive. The assembler inserts the included source text in place of the .include line.

You can specify blocks of source text to be assembled or ignored based on conditions determined during assembly. To delimit text for conditional assembly based on expression evaluations, use the .if, .else, and .endif directives. To delimit text for conditional assembly based on symbol definitions, use the .ifdef, .ifndef, and .ifnotdef directives. These directives are especially useful when used in combination with the D option (described in Chapter 4).

Controlling the Location Counter

The assembler uses the location counter to determine the address of each instruction or data item. The location counter begins at zero and increases by one for each byte assembled. A dot (.) symbolically represents the location counter.

Setting the Location Counter to a Specific Value

To manipulate the location counter directly:

- **.align** increments the location counter to the next address boundary fitting the alignment factor. Also stores the largest alignment found per section into the output file for later use by the linker.

- **.org** sets the location counter to the address you specify.

- **.(dot)** is the location-counter symbol for expressions and assignments.
To align data and instructions, use `.align`. The assembler starts the next instruction or data item on an address that fits the specified alignment, padding the intervening bytes with zeros or with a value you provide.

To set the location counter to a specific address, use `.org` or an assignment statement. The assembler gives the location counter the value you provide. You can express the new address in terms of the current location counter, represented by the dot (`.`). For example, the following advances the location counter by four bytes:

```
.org . + 4
```

The following example uses the location counter (`.`) as an operand behaving just like a local label:

```
lda . , g5
lda . - 4 , g5
lda . + 6 , g7
alab : b blab
blab : cmpojne 0 , 0 , alab
   lda . - alab , g6
.set symname , . - alab
.data
.word .
.word . + 4
.word . - 16
```

### Moving the Location Counter to a Section

In COFF and ELF programs, you can define multiple sections of executable code (text-type sections), initialized data (data-type sections), or uninitialized data (bss-type sections). In b.out-format programs, you can define one `.bss` section, one `.text` text-type section, and one `.data` data-type section. For more information on section types and object-file formats, see the utilities user's guide.
You can start a new section or continue a previous section at any point in your source text with the section directives:

- `.text` puts executable code into a section named `.text`.
- `.data` puts initialized data into a section named `.data`.
- `.bss` puts uninitialized data into a section named `.bss`.
- `.section` for COFF and ELF programs only, puts executable code, initialized data, or uninitialized data into a section that you name.

COFF and ELF programs contain three or more sections; b.out-format programs contain exactly three sections. All object files contain at least the standard `.text`, `.data`, and `.bss` sections.

The order of sections in any program and the names and number of sections in a COFF or ELF program depend on the section definitions in your source text. Omitting the `.text`, `.data`, or `.bss` section directives creates the standard sections with zero size.

The first section directive creates the section and points the location counter to the beginning of the section. Later in the program, you can append text or data to existing sections with additional `.text`, `.data`, or `.bss` section directives or (for COFF and ELF programs) with additional `.section` directives specifying the same section names.

### Initializing Data

To define data in memory, use the data-initialization directives according to the size of the memory block to be initialized and the data format:

- a single memory location with byte, ordinal or integer data
- a single memory location with real data types
- a memory block with string data
- a memory block with specified values or zeros
Initializing Byte, Ordinal, and Integer Data

To initialize data in byte, ordinal, and integer formats, use:

- `.byte` for byte-aligned data (8 bits or shorter).
- `.short`, `.hword` for half-word-aligned data (16 bits or shorter).
- `.int`, `.long`, `.word` for word-aligned data (32 bits or shorter).

You can specify a bit field of up to 32 bits with arguments to the byte-initialization, half-word initialization, and word-initialization directives. For more information, see the Directives Reference on page 5-10.

Initializing Floating-point Data

To initialize data in real or floating-point formats, use:

- `.float`, `.single` for 32-bit real data.
- `.double` for 64-bit real data.
- `.extended` for 80-bit real data (stored in 12 bytes).

How the processor treats real data depends on whether floating-point instructions are supported. The KB and SB include on-chip floating-point support and can use the accelerated floating-point (AFP-960) library. The other i960 processors emulate floating-point arithmetic in software.

For more information on floating-point support, see the AFP-960 library supplement and the processor handbooks.

Initializing String Data

To define character strings, use:

- `.ascii` for a string.
- `.asciz` for a null-terminated string.

For information on characters and escape sequences allowed in character strings, see Chapter 7.
To terminate the string with a null character (ASCII 0), for C language compatibility, use the `.asciz` directive. Using `.ascii` does not append a null character.

You can use `.byte` with a set of character constants in place of `.ascii`. For example, the following assemble the same data:
```
.ascii "cat"        # assemble an ascii string
.byte 'c', 'a', 't'  # assemble 3 ascii bytes
```

## Initializing Blocks of Memory

To put a repeated value into a block of memory, use:
```
.fill        fills the block with a value you specify.
.space       fills the block with zeros.
```

## Defining Symbols

To define symbols, use:
```
.globl, .global  for global symbols in the object-file symbol table.
.comm          for common symbols in the object-file symbol table.
.lcomm         for local common symbols.
.set, .equ, .lsym for non-relocatable symbols.
```

You can make a symbol external implicitly. Using a symbol without defining it adds it to the symbol table as an undefined external symbol. The symbol type and other symbolic information are derived from the context in which you use the symbol.

The assembler uses an internal symbol table that is not retained in the object file. To define and initialize non-relocatable symbols for the internal symbol table, use the `.set`, `.equ`, or `.lsym` directives.
With the optimization and debugging directives, you need use no additional symbol-definition directives. For more information on debugging and optimizing, see the Providing Debugger Information (page 5-8) section and the Optimizing section (page 5-9).

### Providing Debugger Information

For COFF debugging, the compiler puts the following directives in the assembly output:

- **.def** begins a symbol definition.
- **.dim** specifies the array dimensions.
- **.endef** ends a symbol definition.
- **.line** sets a line number.
- **.ln** specifies a line number and the associated address.
- **.scl** declares a storage class.
- **.size** specifies the symbol size.
- **.tag** specifies an associated tag.
- **.type** declares a symbol type.
- **.val** declares the symbol value.

For b.out-format debugging, the compiler puts the following directives in the assembly output:

- **.desc** sets the symbol descriptor.
- **.lsym** creates and initializes a debugging symbol with no additional symbolic information.
- **.stabd** creates a debugging symbol for the location counter.
Directives

.stabn
creates and initializes a debugging symbol named
the empty string ("").

.stabs
creates and initializes a debugging symbol with
all possible symbolic information.

For ELF-format symbol table embellishment, the compiler puts the
following directives in the assembly output:

.elf_size
sets the size of the symbol to the given quantity.

.elf_type
sets the ELF type of the symbol to the given type.

NOTE. For ELF-format object files, the compiler provides debugging
information in DWARF format in separate sections. See the 80960
Embedded ABI (Intel order #631999) for more information on DWARF
format.

For more information on the symbol table, see the i960 Software Utilities
User’s Guide.

Optimizing

To optimize leaf and system procedures, use:

.leafproc
identifies a procedure for branch-and-link
optimization.

.sysproc
identifies a procedure for system-call
optimization.
Marking Position Independence

To mark object files as position-independent, use:

- `.pic` indicates position-independent code.
- `.pid` indicates position-independent data.
- `.link_pix` indicates a position-dependent file intended for linking with position-independent code or data.

Controlling the Listing

When you request a listing, with the `L` command-line option, you can use these directives in the source text:

- `.nolist` turn off listing until the next `.list` directive.
- `.list` turn listing on again after a `.nolist`.
- `.title` specify the listing title.
- `.eject` add a form feed to the listing.

Directives Reference

This section describes the assembly directives alphabetically.

**.ABORT**

*Abort the assembly*

Use `.ABORT` to stop assembly immediately, suppressing the object file.
Example

If `MAX_ERRS` is defined, assembly stops at the `.ABORT` line:

```
ifdef MAX_ERRS
.ABORT
.endif
```

.align

Align the location counter

```
.align align_expr [, data_expr]
```

- `align_expr` specifies the location-counter alignment. This expression is non-relocatable, non-negative, and evaluates to 31 or less.
- `data_expr` optionally specifies a byte value for filling bytes between the old and new location-counter addresses.

Discussion

To align the location counter on byte, word, double-word, or quad-word boundaries, use `.align`. The assembler does the following:

- Increments the location counter to the next value evenly divisible by `2^align_expr`.
- Puts `data_expr` in any unused bytes between the previous and newly aligned location-counter values. Omitting `data_expr` fills the intervening bytes with zeros.
- The align directive also updates the output section’s alignment field in the section header to be the largest alignment per section. This field is used by the linker to enforce alignments of input sections.
When not specified, the default alignments for the following OMFs are as follows:

<table>
<thead>
<tr>
<th></th>
<th>b.out</th>
<th>COFF</th>
<th>ELF</th>
</tr>
</thead>
<tbody>
<tr>
<td>.text</td>
<td>2</td>
<td>0(^{(1)})</td>
<td>2</td>
</tr>
<tr>
<td>.data</td>
<td>0</td>
<td>0(^{(1)})</td>
<td>2</td>
</tr>
<tr>
<td>.bss</td>
<td>0</td>
<td>4(^{(1)(2)})</td>
<td>4</td>
</tr>
<tr>
<td>.section text</td>
<td>NA</td>
<td>0(^{(1)})</td>
<td>2</td>
</tr>
<tr>
<td>.section data</td>
<td>NA</td>
<td>0(^{(1)})</td>
<td>2</td>
</tr>
<tr>
<td>.section bss</td>
<td>NA</td>
<td>4(^{(1)(2)})</td>
<td>4</td>
</tr>
</tbody>
</table>

(1) The COFF assembler emits sections that are multiples of at least 32-bit words. Therefore the smallest default alignment is 2.

(2) The smallest alignment for bss sections in COFF is 4. Anything less is ignored.

Example

The following sets the location counter to 14 hexadecimal and increments it to 18 hexadecimal, the next address evenly divisible by 8 \((2^3)\). The bytes between \(0x14\) and \(0x18\) are filled with zeros.

```
.org 0x14
.align 3
```
Directives

Discussion

To define a character string, use `.ascii` or `.asciz`. The first character occupies the address indicated by the location counter. Successive characters occupy sequential byte locations.

The `.asciz` directive ends the string with a null character; `.ascii` does not. Use a backslash (\) for special characters, as described in Chapter 7.

Examples

1. The following example assembles a string without a null end (13 bytes of information are assembled).
   
   `.ascii "Name\tAddress\n"

2. The following example assembles the same string with a null end (14 bytes of information are assembled).
   
   `.asciz "Name\tAddress\n"

.bss

Identify a symbol for uninitialized data storage

```assembly
.bss name, size_expr, align_expr
```

- `name` is the symbol name.
- `size_expr` specifies a non-negative symbol size, in bytes.
- `align_expr` aligns the symbol. This expression is non-relocatable, non-negative, and evaluates to 31 or less. The assembler assumes a zero alignment if you specify a negative alignment.
Discussion

To create uninitialized symbols, use .bss. The name appears in the symbol table. The assembler extends the .bss section by reserving size_expr bytes, aligned on the next address evenly divisible by align_expr. You can create any number of sections of uninitialized data in a COFF or ELF program. (Use .section name,bss to create another one). You can use any number of .bss directives to extend the .bss section.

For programs with no uninitialized data, the assembler inserts a .bss section of zero size.

Example

The following example, with the location counter starting at 0x14, defines an uninitialized-data symbol named buffer at 0x18, which is the next boundary evenly divisible by 8 (2³). The assembler reserves 256 words (4 bytes each) in the .bss section.

.org 0x14
.bss buffer, 256 * 4, 3

Related Topic

.section

.byte

Assemble byte data

.byte [int_expr:]data Expr [, ...]

int_expr is the number of bits (up to 8) to reserve for the data.

data_expr is the byte value to assemble.
Discussion

To define byte or bit-field data, use `.byte`. The first byte or bit field is byte-aligned on the address indicated by the location counter. Successive bytes and bit fields occupy sequential locations and do not cross byte boundaries.

Each `data_expr` must evaluate to an eight-bit (one-byte) or shorter value. For a bit field shorter than eight bits, specify `int_expr`. The assembler truncates `data_expr` to `int_expr` number of bits. When the bit field cannot fit into the current byte, the assembler pads the current byte with zeros and aligns the bit field on the next eight-bit boundary.

Examples

1. The following allocates three bit fields from the least-significant to the most-significant bit within the byte. No bit field is allocated to the bits marked z, which contain zeros. The first byte is allocated at the address contained in the program counter (pc); the second byte is at the subsequent address (pc + 1).

   `.byte 3:1,2:1,5:1`

   | bit number: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
   | pc          | z | z | z | 0 | 1 | 0 | 0 | 1 |
   | pc + 1      | z | z | z | 0 | 0 | 0 | 0 | 1 |

   Assembling for a big-endian target with the `g` option (see Chapter 4) allocates the bit fields from the most-significant to the least-significant bit within the byte:

   | bit number: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
   | pc          | 0 | 0 | 1 | 0 | 1 | z | z | z |
   | pc + 1      | 0 | 0 | 0 | 0 | 1 | z | z | z |

2. The following assembles three characters:

   `.byte 'a','b','c'`
.comm
Declare a common symbol

.comm name, data_expr [, elf_comm_alignment]
name is the symbol name.
data_expr specifies a non-negative symbol size, in bytes.
elf_comm_alignment In ELF, you can optionally specify the alignment of common symbols.

Discussion
To use a common symbol in more than one module, add the symbol to the object-file symbol table with .comm. Specify the size of the symbol in bytes with the data_expr argument. The assembler creates the symbol as an undefined external type. The linker resolves any references to the symbol from other modules.

The default alignment of a common symbol is determined by the log (base 2) of the size of the symbol:

<table>
<thead>
<tr>
<th>Size</th>
<th>Default Alignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>0,1</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>3,4</td>
<td>2</td>
</tr>
<tr>
<td>5,6,7,8</td>
<td>3</td>
</tr>
<tr>
<td>&gt;= 9</td>
<td>4</td>
</tr>
</tbody>
</table>

When you include a alignment expression, you override the default behavior. The alignment expression is useable only in the ELF assembler.
Examples

The following directives define three common symbols: \texttt{a} occupies four bytes, \texttt{b} occupies two bytes, and \texttt{c} occupies one byte.

\begin{verbatim}
.comm \_a,4
.comm \_b,2
.comm \_c,1
\end{verbatim}

Another example: you have a table of 100 characters, and 100 shorts, and 100 words. You are using the ELF assembler and RAM space is critical so you align them manually:

\begin{verbatim}
.comm chars,100,0
.comm shorts,200,1
.comm words,400,2
\end{verbatim}

\section*{.data}

\textit{Create or extend a data-type section}

\begin{verbatim}
.data
\end{verbatim}

Discussion

To initialize variables, use \	exttt{.data}. When a \texttt{.data} section already exists, this directive sets the location counter to the end of that section.

Omitting \texttt{.data} inserts a \texttt{.data} section of zero size.

Example

The following lines resume or begin the data section of a program:

\begin{verbatim}
.data
.word 0
.double 0d2.5e10
\end{verbatim}
Related Topics

.def, .endef

Provide symbolic information for COFF debugging

.def name

name is the symbol to be described.

Discussion

When you compile a high-level language program for COFF symbolic debugging, the compiler puts symbol descriptions in the assembly output. Such descriptions start with .def and end with .endef.

Example

The following is C language source text:

main() {
  int a;
}

The compiler produces the following symbol description for the debugger. The _a automatic variable appears on the stack 0x40 bytes from the integer frame pointer.

.def _a; .val 0x40; .scl 1; .type 0x4; .endef
Directives

Related Topics

- .dim
- .size
- .val
- .line
- .tag
- .scl
- .type

.desc

Set the symbol descriptor for b.out-format debugging

.desc name, abs_expr

name is the symbol name.

abs_expr evaluates to a non-relocatable value.

Discussion

Compiling a high-level program for b.out-format symbolic debugging adds .desc symbol descriptors as the low-order 16 bits of abs_expr.

.dim

Declare the dimensions of an array for COFF debugging

.dim size_expr [,size_expr [,size_expr [,size_expr]]]

size_expr evaluates to a positive integer for an array dimension.
5

i960 Processor Assembler User's Guide

Discussion

Compiling for COFF symbolic debugging puts symbol descriptions (.def, .endef pairs) for any arrays in the assembly output. The .dim directives specify up to four dimensions for each array.

Related Topics

.double, .doublef, .gendef, .line, .scl

.double

Assemble double-precision (64-bit) floating-point values

.double double_const [, double_const] ...

double_const is a non-relocatable 64-bit floating-point constant, or one of the following:

nan or qnan generates a quiet nan value
snan generates a signalling nan value
+inf generates positive infinity
- inf generates negative infinity

Discussion

To define double-precision floating-point data, use .double. The first value occupies the address indicated by the location counter. Successive values appear in sequential locations. To align the data on particular address boundaries, use the .align directive.
To ensure correct double-precision floating-point evaluation, precede each literal value in the expression with 0d.

Example

The following line assembles the 64-bit value 3.14159:

```
.double 0d3.14159
```

Related Topic

```
.float .extended
```

.eject

*Put a page break into the listing*

Discussion

Use this directive in the source text to insert a page break (formfeed character) in the listing.

Related Topics

```
.list .nolist
.title
```
.elf_size

Adds the given size to the named ELF symbol table entry

.elf_size name, size_expr

Discussion

The .elf_size directive applies only to the ELF assembler. This directive adds the given size to the ELF symbol table. You can view the ELF symbol table with the dumper/disassembler (use [g]dmp960 -t). This information is not used in DWARF.

Example

.text
foo:
lda 0,g0
ret
Lendfoo:
.elf_size foo, Lendfoo - foo

Related Topic

.elf_type
.elf_type

Adds the given type to the named ELF symbol table entry

.elf_type name, { function | object }

Discussion

The .elf_type directive applies only to the ELF assembler. This directive adds the given type to the ELF symbol table entry. You can view the ELF symbol table with the dumper/disassembler (use [g]dmp960 -t). This information is not used in DWARF.

Example

.text
foo:
  lda 0,g0
  ret
Lendfoo:
.elf_size foo, Lendfoo - foo
.elf_type foo, function

Related Topic

.elf_size

.else

See .if
.endif
See .if

.equ, .lsym, .set
Set the value of a symbol

\[
\begin{align*}
&.equ \\
&.lsym \quad name, \ data_expr \\
&.set \quad name, \ data_expr
\end{align*}
\]

name is the symbol name.

data_expr evaluates to a constant during assembly and is assigned to the symbol. The expression must be non-relocatable.

Discussion

To assign a new value to a symbol, use .equ, .lsym, or .set. The value you specify defines or redefines the symbol type.

You may use the same name in more than one .set set per assembly.

A symbol defined with .equ, .lsym, or .set does not appear in the symbol table unless the assembler finds a .global for the symbol name.
Examples

1. The following defines an integer symbol named `useful` with an initial value of 3:
   `.equ useful, 3`

2. The following defines a global symbol named `x`, then specifies `x` as an integer with an initial value of 1:
   `.global x
   .set x, 1`

3. The following sets the temporary symbol `xbase` to 10 and then to 24:
   `.lsym xbase, 10
   .lsym y, xbase
   .lsym xbase, (2*y)+4`

.extended

Assemble extended-precision (80-bit) floating-point data

.extended float_expr [, float_expr]...

`float_expr` is the 80-bit floating-point value to assemble, or one of the following:

- `nan` or `qnan` generates a quiet nan value
- `snan` generates a signalling nan value
- `+inf` generates positive infinity
- `-inf` generates negative infinity
Discussion

To define extended-precision floating-point data, use `.extended`. The first value occupies the address indicated by the location counter. Successive values appear in sequential locations. To align the data on particular address boundaries, use the `.align` directive.

To simplify addressing, the 80-bit floating-point data items defined with `.extended` occupy 12 bytes (96 bits) instead of 10 bytes. The additional two bytes are padded with zeros.

Example

The following line assembles the 80-bit value 3.14159:

```
.extended  3.14159
```

Related Topics

`.double`
`.float`

.file

Identify the source file

```
.file "string"
```

`string` is a source filename, without a pathname. The quotation marks are required.

Discussion

When you compile a high-level language program, the compiler puts a `.file` directive in the assembly source output to identify the primary high-level language source filename. Source debuggers use the `.file` information to identify the original C source file in b.out and COFF.
Directives

Source debuggers using ELF/DWARF obtain source file information from DWARF. However, in ELF, the .file directive modifies the ELF symbol table. You can view the ELF symbol table with the [g]dmp960 -t command.

Example

The following line identifies the source filename as example.c:

.file "example.c"

.fill

Initialize a memory block

.fill int_exp, size_expr, data_expr

int_expr is a non-relocatable expression specifying how many times to repeat the fill data.

size_expr is a non-relocatable expression specifying the size, in bytes, of the fill data (up to eight bytes).

data_expr is a non-relocatable expression specifying the fill data. This expression must evaluate to a byte value.

Discussion

To initialize a memory block with a repeated value, use .fill. The assembler puts data_expr into memory int_expr times, beginning at the current location counter. The memory block occupies (int_expr * size_expr) bytes.

To align the memory block on a particular address boundary, use the .align directive.
Specify the size of \textit{data\_expr} with \textit{size\_expr}, up to eight bytes. When \textit{size\_expr} is larger than needed by \textit{data\_expr}, the excess high-order bytes contain zeros.

**Examples**

1. The following example initializes a memory block of 16 words, filling each word with \texttt{0x0f} (decimal 15).
   \begin{verbatim}
   .fill 16, 4, 2*8-1
   \end{verbatim}

2. The \texttt{.fill} and \texttt{.space} directives are similar. The following lines have identical effects, initializing 4 bytes with the value 1 in each byte:
   \begin{verbatim}
   .fill 4, 1, 1
   .space 4, 1
   \end{verbatim}

**Related Topic**

\texttt{.space}

**.float, .single**

\textit{Assemble single-precision (32-bit) floating-point data}

\begin{verbatim}
{.float } float\_const [, float\_const] ...
{.single} float\_const
\end{verbatim}

\textit{float\_const} is a 32-bit floating-point value to be assembled, or one of the following:

\texttt{nan} or \texttt{qnan} generates a quiet nan value
snan generates a signalling nan value
+inf generates positive infinity
- inf generates negative infinity

Discussion

To define single-precision floating-point data, use .float or .single. The first value occupies the address indicated by the location counter. Successive values appear in sequential locations. To align the data on particular address boundaries, use the .align directive.

Examples

1. The following line assembles the 32-bit value 3.14159:

   .float 3.14159

2. The .float and .single directives have identical effects. The following lines assemble the 32-bit value 3.14159 twice:

   .float 3.14159
   .single 3.14159

Related Topics

.double
.extended

.global, .globl

Declare a global symbol

.global name
.globl name

name is the name of the external symbol.
Discussion

To make the defined symbol \textit{name} an external symbol, use \texttt{.globl} or \texttt{.global}. The linker resolves any references to the symbol from other modules.

Example

The following example makes the label \texttt{_exit} a global symbol:

\begin{verbatim}
.globl _exit
\end{verbatim}

\texttt{.hword}

\textit{See .short}

\texttt{.ident}

\textit{Include identification, date, and time in the object file}

\begin{verbatim}
.ident ident_str[, time_value]
\end{verbatim}

\texttt{ident_str} identifies the compiler.

\texttt{time_value} is the time value returned by the \texttt{time} function.
Discussion

To put compiler information in the symbol table, use the `.ident` directive and the `I960IDENT` environment variable. Add an identification string with `ident_str`. Put a specific time and date in the symbol table with `time_value`. Omitting `time_value` puts the assembly time and date in the symbol table.

Assembly language output from the compiler includes a `.ident` line.

Example

The following identifies the compiler at 10:20, 13 November, 1991:

```
.ident "iC960 V4.0X, 0x29216cde"
```

`.if, .ifdef, .ifndef, .ifnotdef, .else, .endif

Identify blocks of source text for conditional assembly

```
{.if cond_expr
  {.ifdef
    {.ifndef
      .ifnotdef
    }
  }
  stmt_block [.else stmt_block]
}.endif
```

- `cond_expr` evaluates to a non-relocatable constant during assembly. The condition is false when `cond_expr` is zero and true otherwise.
- `symbol` is a symbol name.
- `stmt_block` is a block of one or more assembly statements.
Discussion

To conditionally assemble a block of source text, begin the block with `.if`, `.ifdef`, `.ifndef`, or `.ifnotdef` and end the block with `.endif`. The assembler selects the block to assemble as follows:

- with `.if` when `cond_expr` is non-zero
- with `.ifdef` when `symbol` is defined
- with `.ifndef` when `symbol` is not defined
- or `.ifnotdef`
- with `.else` when the preceding `.if`, `.ifdef`, `.ifndef`, or `.ifnotdef` block is not selected

The `.else` directive ends an `.if`, `.ifdef`, `.ifndef`, or `.ifnotdef` block and the `.endif` directive ends any conditional-assembly block. You can nest conditional-assembly blocks.

These directives are best used in combination with the `D` option (described in Chapter 4).

Example

The following code assembles a double-precision floating-point value when `UseDouble` is nonzero and a single-precision floating-point value otherwise:

```
.if UseDouble
  .double 3.14159
.else
  .float 3.14159
.endif
```
Directives

.include

Insert source text from a file

.include "filename"

filename is the include filename. The quotation marks are required.

Discussion

To insert source text from a file, use the .include directive. The contents of the included file are assembled in place of the .include statement.

To include a file from elsewhere than the current directory, you can:

• provide the complete pathname for the file
• use the I option (described in Chapter 4)
• define the I960INC or G960INC environment variable (described in Chapter 3).

Example

The following includes the source files gen_d.asm and gen_e.asm in the stdin input:

asm960 -i
.equ UseDouble, 1
.include "gen_d.asm"
.ifdef D_ERR
.ABORT
.endif
.include "gen_e.asm"
^d
.int

See .word

.lcomm

Declare a local common symbol

.lcomm symbol, size_expr

symbol

names the symbol.

size_expr

evaluates to the length, in bytes, of the symbol.

Discussion

To declare a local common symbol, use the .lcomm directive. The assembler allocates space in the .bss (uninitialized-data) section for the symbol. The symbol appears in the symbol table as static.

Example

The following declares a 4-byte (1-word) local common symbol named mycom:

.lcomm mycom, 4
.leafproc

Declare a leaf procedure

.leafproc name[, bal_entr]

name is the leaf procedure name, as used in the high-level-language procedure reference.

bal_entry is the branch-and-link entry-point label.

Discussion

You can optimize some procedure calls by substituting branch-and-link (bal or balx) instructions for call (call or callx) instructions. Identify such procedures with .leafproc. Specify the call entry point with name and the branch-and-link entry point with bal_entry.

A leaf procedure must meet the following requirements:

- The procedure must use registers minimally. Available registers are g0 through g7 for the first eight words of an argument list, g8 through g11 for an additional four words, and g13.
- The procedure can call no other procedures.
- The procedure can have no stack requirements, because no stack frame is allocated for leaf procedures.
- The procedure can have no argument block because register g14 contains the calling-procedure return address.
- The procedure cannot accept a variable argument list.

A leaf procedure has two entry points. The entry point for call instructions must provide a return sequence (prolog and epilog). The entry point for branch-and-link instructions must skip the return sequence.
When you compile a high-level language program for leaf-procedure optimization, the compiler identifies the leaf procedures, inserts the \texttt{.leafproc} directives, and generates the calling-convention blocks. For the call entry point, the compiler adds a single underscore (\_) to the beginning of the procedure name. For the branch-and-link entry point, the compiler appends the suffix \texttt{.lf}.

If you don't specify a branch-and-link entry point, the assembler assumes that the branch-and-link entry point and the name entry point are the same.

**Example**

Compiling the following C source code produces the \_\_\_add\_\_ entry point:

```c
int add(a, b)
int a,b;
{
    return(a+b);
}
```

The resulting assembly code is:

```
.align 4
.def __add; .val __add; .scl 108; .type 0x44; .endef
.globl __add
.leafproc __add, add.lf
__add:   lda LR2, g14
add.lf:  mov g14, g7
           addi g0, g1, g0
           mov 0, g14
           bx  (g7)
LR2 ret .ln 3
```

The \texttt{.scl 108} storage-class indicates an external leaf procedure. The \_\_\_add\_\_ is the call entry point. The \_\_add\_\_.lf is the branch-and-link entry point.

Since this example is compiled for source debugging, the compiler adds the \texttt{.def} directives.
Directives

5-37

5

Identify the line number of a COFF debugging symbol

.line int_expr

int_expr evaluates to a positive integer to be used as a line number.

Discussion

Compiling for COFF source debugging puts .line directives in the symbol definitions (.def, .endef pairs). The int_expr is the line number for the line defining the symbol declared in the .def block.

Related Topics

.def .ln .ndef

.link_pix

See .pic
.list
Re-enable listing after a .nolist

.list

Discussion
Listing resumes on the instruction or directive immediately following this directive. This option is useful in combination with .nolist when you want to list only part of the source text.

Related Topics
.nolist .title .eject

.In
Specify a line number within a function

.ln int_expr [, addr_expr]

int_expr evaluates to a positive integer to be used as a line number.

addr_expr is the address of a line.
Discussion

Compiling for source debugging puts `.ln` directives in the source text to reset the source line numbers relative to the beginning of functions.

The assembler numbers the line containing the `.ln` directive as `int_expr` and the subsequent line as `(int_expr + 1)`. Omitting `addr_expr` uses the location counter (`.`).

The `.ln` directive appears outside of any debugging symbol definition (.def,.endef pair).

Example

The following specifies line number 10 for the current position of the location counter:

```
.ln 10, .
```

Related Topic

`.line`

.lomem

Generate short memory-access instructions

```
.lomem name
```

`name` identifies a symbol.
Discussion

This directive identifies a symbol’s address as falling within the range 0 - 0xfff. This is the range of addresses that can be reached with the absolute offset of a MEMA format instruction. The assembler uses MEMA format for all MEM format instructions that reference the symbol. This yields a space savings of 4 bytes per instruction over MEMB format.

The symbol’s .lomem declaration must appear before the first use of the symbol in a MEM format instruction. Otherwise the assembler defaults to MEMB format.

To declare an entire section’s symbols “lomem” use the .lomem attribute to the .section directive.

Example

The following example declares the symbol foo to be “lomem” and then loads its contents into a register. The ld instruction that follows is 4 bytes long.

foo: .lomem foo
ld foo, r4

Related Topic

.section

.long

See .word
.lsym

See .equ

.nolist

Turn listing off

Discussion
Listing stops immediately, and does not resume again until a .list directive is seen. This option is useful in combination with .list when you want to list only part of the source text. The assembler ignores this directive when you use the La option on the command line.

Related Topics
.list .title
.eject

.org
Set the location counter

.org addr_expr[, abs_expr]

addr_expr is an integer expression.

abs_expr is a non-relocatable byte value to be used as a fill value.
Discussion

To point the location counter to a specific address, relative to the start of the current segment, use `.org`. Specify the new address with `addr_expr`. The assembler puts zeros in the bytes between the old and new addresses. You can specify a value other than zero with `abs_expr`. The assembler does not issue a warning for large `addr_expr` values. Note that such use can fill up a hard disk quickly.

Example

The following example advances the location counter (.) by four bytes:

```
.org . + 4
```

Related Topics

```
.align .section
.bss .text
.data
```

.pic, .pid, .link_pix

Mark the object file as compatible with position-independent modules

```
{.link_pix}
{.pic
{.pid
```
Discussion

For position-independent programs, you must ensure consistent position independence of the object code and data across the object files. The linker examines each object file header and issues warning messages for mismatches. To suppress the warning messages, put one of the following directives at the beginning of your source text:

- `.pic` indicates a file containing position-independent code.
- `.pid` indicates a file containing position-independent data.
- `.link_pix` indicates compatibility with position-independent code, data, or both.

For more information on position independence, see your compiler manual.

.scl

*Declare the storage class for COFF symbolic debugging*

`.scl int_expr`

`int_expr` evaluates to a positive integer indicating the storage class.

Discussion

Compiling for COFF symbolic debugging puts symbol descriptions (`.def`, `.endef pairs`) in the assembly output. The `.scl` directives specify the storage class for each symbol so described.
Example

The following example specifies the 113 storage class, indicating a static leaf procedure, for the add procedure:

```
.def _add; .val _add; .scl 113; .type 0x44; .endef;
```

Related Topics

```
.def .dim .line .size .tag .type .val
```

.section

*Creates or extends a COFF or ELF program section*

```
.section name, [, attribute_list]
```

- `name` identifies the section.
- `attribute_list` identifies the attribute(s) associated with this section.

Discussion

To create or extend a program section that you name, use `.section`. When the named section already exists, `.section` sets the location counter to the end of the named section. You can create multiple sections of instructions (text-type) or initialized data (data-type) or uninitialized data (bss-type) in a COFF or ELF program but not in a b.out-format program.
You can have any number of attributes for any given section. Attributes can be duplicated. An empty attribute list is allowed and means the section does not have any of the attributes. The attributes apply to both COFF and ELF unless otherwise indicated. If a COFF-only attribute is given to the ELF assembler, it is silently ignored and vice versa.

The attributes and their effects are:

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>alloc</td>
<td>The section should cause the linker to allocate memory (e.g., DWARF sections are not allocated).</td>
</tr>
<tr>
<td>bss</td>
<td>The named section takes on the same attributes as the .bss section.</td>
</tr>
<tr>
<td>data</td>
<td>The named section takes on the same attributes as the .data section.</td>
</tr>
<tr>
<td>exec</td>
<td>The named section contains executable code.</td>
</tr>
<tr>
<td>info</td>
<td>The section contains information only. (COFF only)</td>
</tr>
<tr>
<td>lomem</td>
<td>The named section is intended to be located in low memory. References to labels in this section will be via MEMA format instructions. (See .lomem for more information about MEMA format instructions.)</td>
</tr>
<tr>
<td>msb</td>
<td>The section is generated in big-endian byte order. (ELF only)</td>
</tr>
<tr>
<td>pi</td>
<td>The named section is position independent. (ELF only)</td>
</tr>
<tr>
<td>read</td>
<td>The section contains readable memory. (ELF only)</td>
</tr>
<tr>
<td>super_read</td>
<td>The memory space where the section resides corresponds to memory that is readable, writeable, or executable when the processor is in supervisor mode only. (ELF only)</td>
</tr>
<tr>
<td>super_write</td>
<td>The memory space where the section resides corresponds to memory that is readable, writeable, or executable when the processor is in supervisor mode only. (ELF only)</td>
</tr>
<tr>
<td>super_exec</td>
<td>The memory space where the section resides corresponds to memory that is readable, writeable, or executable when the processor is in supervisor mode only. (ELF only)</td>
</tr>
<tr>
<td>text</td>
<td>The named section takes on the same attributes as the .text section.</td>
</tr>
<tr>
<td>write</td>
<td>The section contains writeable memory. (ELF only)</td>
</tr>
</tbody>
</table>
Note that for the `super_read`, `super_write`, and `super_exec` attributes, the assembler ORs the following bits into the corresponding section header flag word: `SHF_960_SUPER_READ`, `SHF_960_SUPER_WRITE`, `SHF_960_SUPER_EXECINSTR`. See the 80960 ABI specification (Intel order #631999) for more information. The linker passes these bits on from input files to the output file, ORing all of the flagwords together. The runtime does not ensure that these semantics are enforced. These bits are here for convenience, and to let you specify code bound for supervisor mode.

**Example**

The following lines begin a data section named `sram` that is bound for low memory, create another data section named `mydata` that is position-independent, and then continue `sram`:

```
.section sram, data, lomem
.globl _a
_a: .space 4
.section mydata, data, pi
.globl _b
_b: .word 444
.section sram, data
.globl _d
_d: .word 44
```

**Related Topics**

`.bss`      `.text`
`.data`      `.lomem`

**.set**

*See .equ*
.short, .hword

Assembles 16-bit data

\[
\text{.short} [\text{int}_\text{expr}] \text{ data}_\text{expr} [, \ldots]
\]

\text{int}_\text{expr} \quad \text{is the bit-field length, up to 16 bits.}

\text{data}_\text{expr} \quad \text{is a 16-bit value to be assembled.}

Discussion

To define half-word or short-integer data, use the .short or .hword directive. The first value occupies the address specified by the location counter. Successive values occupy sequential two-byte locations. To align the data on particular address boundaries, use the .align directive.

For a bit field, specify the number of bits with \text{int}_\text{expr}. The assembler truncates the \text{data}_\text{expr} value to \text{int}_\text{expr} number of bits. When the bit field cannot fit into the current half-word, the assembler fills the remaining bits of the current half-word with zeros and begins the bit field on the next 16-bit boundary.

Examples

1. The .short and .hword directives have identical effects. The following assembles two half-words of data:

   \text{.hword} \ 0\text{xFEFE}
   \text{.short} \ 0\text{xEFEE}

2. The following allocates three bit fields from the least-significant to the most-significant bit within the half-word. No bit field is allocated to the bits marked \( z \), which contain zeros. The first half-word is allocated at the address contained in the program counter (pc); the second word is at the subsequent address (pc + 2).

   \text{.hword} \ 3:3, 6:62, 9:21
Assembling for a big-endian target (with the G option) allocates the bit fields from the most-significant to the least-significant bit within the byte:

<table>
<thead>
<tr>
<th>bit number:</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>pc</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>pc + 1</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>1</td>
</tr>
<tr>
<td>pc + 2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>pc + 3</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>0</td>
</tr>
</tbody>
</table>

Related Topics

- `.ascii`
- `.asciiz`
- `.byte`
- `.double`
- `.float`
- `.int`
- `.long`
- `.octa`
- `.quad`
- `.single`
- `.word`

**.single**

See `.float`
.size

Declare the size of a symbol for COFF debugging

.size size_expr

size_expr is the size of a symbol, up to 64 kilobytes (65535 in decimal or 0xFFFF in hexadecimal). The expression must evaluate to a positive integer.

Discussion

Compiling for COFF symbolic debugging puts symbol descriptions (.def, .endef pairs) in the assembly output. The .size directive defines the size of a symbol so described. For structures and arrays, .size specifies the total extent of the symbol.

Due to COFF limitations, specifying too large a symbol size generates invalid debug information.

Related Topics

.def  .line  .type
.dim   .scl   .val
.endef  .tag
.space

Initialize a memory block with byte values

.space size_expr[, data_expr]

size_expr is the number of bytes to be initialized. The expression must evaluate to a positive integer.

data_expr is a byte value to be put repeatedly into the memory block.

Discussion

To increment the location counter and initialize the intervening bytes, use .space. This directive advances the location counter by size_expr bytes and fills the bytes between the old and new locations with the data_expr value. Omitting data_expr fills the intervening bytes with zeros.

Examples

1. The following example initializes 64 bytes with zeros:
   .space 16 * 4
2. The .fill and .space directives are similar. Using .space has the same effect as using .fill with a data size of 1 byte. The following lines have identical effects, initializing 4 bytes with the value 1 in each byte:
   .fill 4, 1, 1
   .space 4, 1

For more examples, see Chapter 9.

Related Topic

.fill
.stabd, .stbn, .stabs

Create b.out-format debugging symbols

.stabd type, other, desc
.stabn type, other, desc, value
.stabs name, type, other, desc, value

- **name**: is the new symbol name, with any characters except \000.
- **value**: is a non-relocatable expression initializing the symbol.
- **type**: is a non-relocatable expression for the symbol type.
- **other**: is a non-relocatable expression.
- **desc**: is a non-relocatable expression for the symbol descriptor.

**Discussion**

For symbolic debugging, you can create symbols that cannot be referenced by name during assembly. Such symbols can have the following attributes:

- **value**: To record the location counter during assembly, define a symbol with .stabd. For any other initial value, use .stbn, or .stabs.
- **type**: Provide the symbol type as the low-order eight bits of a non-relocatable expression.
- **name**: Since the symbol name can contain almost any character, a debugger can use this field for additional information.
The debugger can use this attribute for any purpose. For .stabd, .stabn, and .stabs, provide the initial other value as the low-order eight bits of a non-relocatable expression.

Provide the symbol descriptor as the low-order 16 bits of a non-relocatable expression.

**.sysproc**

*Declare a system procedure*

```assembly
.sysproc name, int_expr
```

*name* is the procedure name.

*int_expr* is the system-procedure table index. The expression must evaluate to an integer between zero and 259, inclusive.

**Discussion**

To use the i960 processor system-call feature, identify functions as system procedures with the *sysproc* directive. You need specify any function as a system procedure only once in your program.

Assign each system procedure an *int_expr* index number in the system procedure table, as follows:

- For b.out-format programs, the index must be between 1 and 253, inclusive.
- For COFF and ELF programs, the index must be between zero and 259, inclusive.

If you don't provide an index number, the assembler assigns the special index number -1. This number tells the linker to look for the real index number in another module. You must supply the real index number in at least one assembly source file or your application will not link.
Directives

For more information on system calls and the system procedure table, see your processor manual.

**Example**

The following example specifies `_add` as a system procedure with an index of 29:

```
.align  4
.globl  _add
.sysproc _add, 29
_add:
    addi g0, g1, g0
    ret
.ln  3
```

**Related Topic**

`.leafproc`

---

**.tag**

_Declare a tag for a COFF debugging symbol_

```
.tag string
```

*string* is the symbol name.

**Discussion**

Compiling for COFF symbolic debugging puts symbol descriptions (.def, .endef pairs) in the assembly output. References from within a symbol-description block to a previous block use the `.tag` directive. The *string* is the name of the symbol defined in the previous block.
In a structure or union symbol-description block, the .tag identifies a structure or union defined in a previous block.

**Related Topics**

- .def
- .dim
- .endef
- .line
- .scl
- .size
- .type
- .val

**.text**

*Create or extend a text-type section*

```
.text
```

**Discussion**

To create a program section for instructions, use the .text directive. If a .text section already exists, this directive sets the location counter to the end of that section. Omitting .text inserts a .text section of zero size.

**Example**

The following lines resume or begin the .text section of a program:

```
.text
mov r3, r4
ldconst 0xff, g5
```

**Related Topics**

- .bss
- .section
- .data
.title
Specify the listing title

.title "string"
string is the title you want to appear in the listing. The quotation marks are required.

Discussion
Use this directive anywhere in the source text to specify the listing title. Only the first such directive has meaning. This directive is ignored when you also give the Lt command-line option.

Related Topics
.list .nolist .eject

.type
Declare the COFF debugging-symbol type

.type int_expr
int_expr evaluates to a positive integer specifying a COFF type.

Discussion
Compiling for COFF symbolic debugging puts symbol descriptions (.def, .endef pairs) in the assembly output. The .type directive adds type information to the symbol description.
5

Related Topics

- .def
- .dim
- .endef
- .line
- .scl
- .size
- .tag
- .val

.val

Declare a debugger-symbol value

.val data Expr

data Expr is the value of the symbol.

Discussion

Compiling for COFF symbolic debugging puts symbol descriptions (.def, .endef pairs) in the assembly output. The .val directive initializes the symbol.

Example

The following example shows .val and other debugging directives in a symbol-description block describing the myfcn function:

myfcn:
.def myfcn; .val myfcn; .scl 2; .type 0x44; .endef

Related Topics

- .def
- .dim
- .endef
- .line
- .scl
- .size
- .tag
- .type
.word, .int, .long

Assemble word data

```
[int_expr:] data_expr[, ...]
```

- **int_expr** is the length of the data field, up to 32 bits.
- **data_expr** is the 32-bit integer value to be assembled.

Discussion

To define word-aligned integer, word, or bit-field data, use .int, .long, or .word. The first value occupies the address specified by the location counter. Successive values occupy sequential locations. To align the first value on a particular address boundary, use the .align directive.

For a bit field, specify the number of bits with *int_expr*. The assembler truncates the *data_expr* value to *int_expr* number of bits. When the bit field cannot fit into the current word, the assembler fills the remaining bits of the current word with zeros and begins the bit field on the next 32-bit boundary.

Examples

1. The .int, .long, and .word directives have identical effects:
   ```
   .int 5
   .long 5
   .word 5
   ```

2. The following allocates three bit fields from the least-significant to the most-significant bit within the word. No bit field is allocated to the bits marked z, which contain zeros. The first word is allocated at the address contained in the program counter (pc); the second word is at the subsequent address (pc + 4).
   ```
   .int 16:1,10:1,8:1
   ```
Assembling for a big-endian target (with the G option) allocates the bit fields from the most-significant to the least-significant bit within the byte:

<table>
<thead>
<tr>
<th>bit number:</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>pc</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>pc + 1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>pc + 2</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>pc + 3</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>pc + 4</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>pc + 5</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
</tr>
<tr>
<td>pc + 6</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
</tr>
<tr>
<td>pc + 7</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
<td>z</td>
</tr>
</tbody>
</table>

Related Topics

- `.ascii`
- `.asciiz`
- `.byte`
- `.double`
- `.extended`
- `.float`
- `.hword`
- `.short`
- `.single`
Assembler error and warning messages appear on stderr as:

[source:] [n]: message

- source is the source filename.
- n is the line number of the error, appearing only for source-assembly errors. File, I/O, and command-line errors do not have source line numbers.
- message is the text of the message.

Error messages report file-specification or syntax errors during assembly. In addition to producing a message, the assembler acts on the severity of the error as follows:

- For fatal errors, assembly stops. No object file is produced.
- For non-fatal errors, assembly continues to the end of the input, but no object file is produced.
- For warnings, assembly continues and an object file is produced.
Assembly Language

This chapter provides:

• an overview of assembly language directive and instruction syntax
• a description of the assembly language elements
• a description of the assembly language statement syntax

Assembly Language Statement Format

Assembly language source is a sequence of statements separated with newline characters or semicolons. A valid assembly language statement follows this syntax:

[label] [keyword] [operands]

A keyword can be any of the following:

Directives affect the assembly, as explained in Chapter 5.

Instructions specify processor operations.

Pseudo-instructions (also called pseudo operations) are replaced with machine instructions by the assembler or linker.

You can write null statements, including empty lines and lines with only a semicolon. For null statements, the assembler generates no machine code, allocates no storage, and does not change the location counter.

A statement can contain one or more labels. Place labels before instruction keywords, as described in the Labels section of this chapter. One or more operands can follow the keyword, as needed.
Lexical elements are the building blocks of assembly language statements, used to construct labels, keywords, and operands. The lexical elements supported by the assembler are:

- the character set
- tokens and separators
- identifiers
- constants
- labels
- operators
- expressions
- comments

### Character Set

The character set used in assembly language programming is a subset of the ASCII character set. Table 7-1 shows the valid character set.

<table>
<thead>
<tr>
<th>Characters</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABCDEFGHIJKLMNOPQRSTUVWXYZ</td>
<td>alphabetic, UPPERCASE</td>
</tr>
<tr>
<td>abcdefghijklmnopqrstuvwxyz</td>
<td>alphabetic, lowercase</td>
</tr>
<tr>
<td>0123456789</td>
<td>numbers</td>
</tr>
<tr>
<td>+ - * / ( ) [ ] &lt; &gt; ; : . &quot; _ : ? @ &amp; #</td>
<td>special characters</td>
</tr>
<tr>
<td>\</td>
<td>delimiters</td>
</tr>
</tbody>
</table>

1 In Windows, a newline is a carriage return-linefeed combination while on UNIX it is a linefeed only.

The assembler is case-sensitive. You can write labels and comments in uppercase or lowercase, but references to a label must match the case in the label definition. For example, the label `zz` is different from the label `zz`. Instruction mnemonics and most directives use only lowercase characters.
Tokens and Separators

The assembler processes statements constructed of tokens and separators. Assembly language tokens include identifiers (symbols or names), constants, operators, and keywords.

The keywords are directives, instruction mnemonics, and pseudo-instructions. Statement syntax depends on the keyword. Directives are described in Chapter 5. Machine instructions are described in this chapter briefly, and in greater detail in the processor user’s manuals. Pseudo-instructions are described in Chapter 8.

Separate identifiers or constants with at least one blank space or tab character. You can also use a blank or tab to separate other tokens such as operators or keywords. Put no blanks or tabs within tokens.

Identifiers

An identifier is a sequence of alphanumeric characters, including the underscore (\_), dollar sign ($), and period (.). The first character in an identifier must not be numeric. Identifiers can have up to 255 significant characters.

Constants

There are three kinds of constants: simple, character, and string.

Simple Constants

Simple constants are either numeric or single-character. The digits in numeric constants are:

0123456789
abcdef
ABCDEF
Digits 0 through 9 represent corresponding numeric values, depending on the current number base (octal, decimal, or hexadecimal). The digits a, b, c, d, e, and f are identical to A, B, C, D, E, and F, representing hexadecimal values corresponding to the decimal values 10 through 15. Integer and ordinal constants are 32-bit-wide, two's-complement numbers.

The following types of constants are formed:

- **octal**: An octal constant is a sequence of the digits 0 through 7 with a leading 0. For example, 012 represents decimal 10.
- **decimal**: A decimal constant is a sequence of the digits 0 through 9 without a leading 0. For example, 10 represents decimal 10.
- **hexadecimal**: A hexadecimal constant is a sequence of the digits 0 through 9, a, b, c, d, e, f, or A, B, C, D, E, F with a prefix of 0x or 0X. For example, 0x1a represents the decimal value 26.
- **floating-point**: A floating-point constant consists of one or more characters that the C library function `atof` recognizes as a floating-point number, preceded by an optional prefix listed in Table 7-2.

### Representing Floating-Point Numbers

All floating-point constants are represented according to the *IEEE Standard for Binary Floating-point Arithmetic*.

#### Table 7-2 Prefixes for Floating-point Constants

<table>
<thead>
<tr>
<th>Prefix</th>
<th>Used for</th>
</tr>
</thead>
<tbody>
<tr>
<td>0f or 0F</td>
<td>Single-precision value, 32 bits</td>
</tr>
<tr>
<td>0d or 0D</td>
<td>Double-precision value, 64 bits</td>
</tr>
<tr>
<td>0e or 0E</td>
<td>Extended-precision value, 80 bits</td>
</tr>
</tbody>
</table>
The characters e, E, d or D designate the exponent field. You can use only .0 and 0.0 as floating-point literals with numerics instructions, as shown in Table 7-3.

### Table 7-3 Floating-point Literals

<table>
<thead>
<tr>
<th>Representation</th>
<th>Value Assembled</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.0</td>
<td>0f+0.0</td>
</tr>
<tr>
<td>1.0</td>
<td>0f+1.0</td>
</tr>
</tbody>
</table>

Example 7-1 uses numeric constants and literal values in assembly language instructions.

### Example 7-1 Example of Constants and Literal Values

```markdown
/* example of numeric constants */
mov 31,g5           /* decimal */
mov 037,g5         /* same in octal */
mov 0x1f,g5       /* same in hex */
movr 0.0,g5        /* float literal */
movrl 0f1.0,g4     /* float literal */
addr 0.0,1.0,g0    /* together */
```

### Character Constants

A single-character constant is an ASCII character enclosed within apostrophes ('). (The apostrophe is ASCII decimal character 39.)

The value of an ASCII character constant is either the ASCII code for the character or the C language interpretation of an escape sequence, beginning with a backslash, as shown in Table 7-4.
Table 7-4  Character Constants

<table>
<thead>
<tr>
<th>Escape Sequence</th>
<th>Interpretation</th>
</tr>
</thead>
<tbody>
<tr>
<td>\b</td>
<td>backspace</td>
</tr>
<tr>
<td>\f</td>
<td>form feed</td>
</tr>
<tr>
<td>\n</td>
<td>new-line</td>
</tr>
<tr>
<td>\r</td>
<td>carriage return</td>
</tr>
<tr>
<td>\t</td>
<td>horizontal tab</td>
</tr>
<tr>
<td>\v</td>
<td>vertical tab</td>
</tr>
<tr>
<td>\</td>
<td>backslash</td>
</tr>
<tr>
<td>\</td>
<td>backslash</td>
</tr>
<tr>
<td>'</td>
<td>apostrophe</td>
</tr>
<tr>
<td>&quot;</td>
<td>quotation mark</td>
</tr>
<tr>
<td>\octal constant</td>
<td>ASCII value of constant</td>
</tr>
</tbody>
</table>

String Constants

A string constant has the same syntax and semantics used in the C language. Each string begins and ends with a quotation mark (" ). All C language conventions for the backslash are observed. See Table 7-4 for a summary.

Strings are identified by value and length. However, the assembler does not implicitly end strings with a null byte, unlike the C compiler. For information on adding ASCII string data to your assembly files, see the .ascii and .asciz directive entries in Chapter 5.

Labels

A label is a symbol with a location counter value and type. The assembler recognizes the following kinds of labels:

- **global**: is an alphanumeric identifier, also called a name.
- **local**: is a single decimal digit (0 to 9), also called a numeric label.
Global labels are uniquely defined and remain in the output symbol table unless the label name begins with a period (.) or an L. Labels beginning with a period (.) or an L can be included in the symbol table by using the assembler –d option. See Chapter 4 for more information.

Name (Global) Labels

A global label consists of an identifier followed by a colon (:). In effect, a name label assigns the current value and section (e.g., .text or .data) of the location counter to the name. A global label is referenced by its name. Global labels beginning with a dot (.) or an L are discarded from the output symbol table, unless you use the –d option.

The assembler generates an error if a symbol is multiply defined.

Numeric (Local) Labels

A numeric label consists of a digit 0 to 9 followed by a colon (:). Numeric labels define temporary symbols of the form nb and nf, where n is the numeric digit of the label. References to symbols of the form nb refer to the first numeric label n: backward from the reference; nf symbols refer to the first numeric label n: forward from the reference.

As with global labels, a numeric label assigns the current value and section (e.g., .text or .data) of the location counter to a symbol. Unlike global symbols, which you can define only once within an assembly, numeric labels are local symbols. Therefore, programs can define several identical numeric labels (the same digit) within an assembly.

Expressions

An expression is a sequence of symbols representing a calculated value. An expression can consist of identifiers, constants, operators, and other expressions. Each expression has a type. Expressions can be grouped by enclosing them within parentheses.
Integer quantities appearing in arithmetic expressions are represented internally as two's-complement numbers with 32-bit precision. You can add only one forward-referenced external symbol to an expression. Further, you can subtract only one forward-referenced external symbol from an expression. The exception to these rules is that the difference expression of backwards-reference external symbols in the same section is treated as a constant value (see Example 7-2).

Example 7-2  Forward-reference External Symbol in Expressions

```assembly
/* LEGAL: Forward (+) Reference to a symbol */
.word _label
/* LEGAL: A single (+) and single (-) forward reference */
_label4:
_label5:
.word _label7 - _label6
_label6:
_label7:
/* LEGAL: The difference expression of two labels in the * same section is treated as a constant, allowing for * other (+) or (-) references, up to 1 each maximum. */
.word (_label5 - _label4) + (_label7 - _label6) - _label8 + _label9
```

Operators

The assembler recognizes certain operators that you can use to form valid expressions. These operators and the operations they represent appear in Table 7-5.
### Table 7-5 Expression Operators

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>+</td>
<td>addition</td>
</tr>
<tr>
<td>-</td>
<td>subtraction</td>
</tr>
<tr>
<td>*</td>
<td>multiplication</td>
</tr>
<tr>
<td>/</td>
<td>division</td>
</tr>
<tr>
<td>%</td>
<td>modulo</td>
</tr>
<tr>
<td>&amp;</td>
<td>bitwise and</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>~</td>
<td>one's complement</td>
</tr>
<tr>
<td>^</td>
<td>bitwise exclusive or</td>
</tr>
<tr>
<td>&gt;&gt;</td>
<td>logical right shift</td>
</tr>
<tr>
<td>&lt;&lt;</td>
<td>logical left shift</td>
</tr>
<tr>
<td>&lt;= &gt; &gt;=</td>
<td>less than, less than or equal to, greater than, greater than or equal to</td>
</tr>
<tr>
<td>== ! =</td>
<td>equals, not equals</td>
</tr>
<tr>
<td>&amp;&amp;</td>
<td>logical and, does not short circuit</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>!</td>
<td>la == if (a) then 0 else 1; (logical negation)</td>
</tr>
</tbody>
</table>

In Table 7-6, operators are listed in order of precedence from highest to lowest.

### Table 7-6 Operator Precedence

<table>
<thead>
<tr>
<th>Type</th>
<th>Operators</th>
</tr>
</thead>
<tbody>
<tr>
<td>unary</td>
<td>~, +, !, ~</td>
</tr>
<tr>
<td>binary</td>
<td>*, /, %</td>
</tr>
<tr>
<td>binary</td>
<td>+, -</td>
</tr>
<tr>
<td>binary</td>
<td>&lt;&lt;, &gt;&gt;</td>
</tr>
</tbody>
</table>
## Table 7-6  Operator Precedence (continued)

<table>
<thead>
<tr>
<th>Type</th>
<th>Operators</th>
</tr>
</thead>
<tbody>
<tr>
<td>binary</td>
<td>&lt;, &lt;=, &gt;, &gt;=</td>
</tr>
<tr>
<td>binary</td>
<td>==, !=</td>
</tr>
<tr>
<td>binary</td>
<td>&amp;</td>
</tr>
<tr>
<td>binary</td>
<td>^</td>
</tr>
<tr>
<td>binary</td>
<td></td>
</tr>
<tr>
<td>binary</td>
<td>&amp;&amp;</td>
</tr>
<tr>
<td>binary</td>
<td></td>
</tr>
</tbody>
</table>

All binary operators with the same precedence are evaluated from left to right in the expression, except for any evaluation order enforced by parentheses.

## Expression Types

The assembler deals with several types of symbols and expressions. The assembler recognizes the following expression types:

**absolute**  
An absolute symbol is defined ultimately from a constant. Applying the linker to the output file does not affect the value of absolute symbols or expressions.

**bss**  
The value of a .bss symbol is measured as the number of bytes from the beginning of the .bss section of a program. Like .text and .data symbols, the value of a .bss symbol can change on different linker runs.

**data**  
The value of a .data symbol is measured as the number of bytes from the origin of the .data section. Like .text symbols, the value of .data symbols can change on different linker runs. After the first .data statement, the value of the location counter 0 of the .data section.
| **external absolute text, data, or bss** | Symbols can be declared as `.globl` but defined within an assembly as absolute `.text`, `.data`, or `.bss` symbols. These symbols are used exactly as if they were not declared as globals. However, their value and type are available to the linker so that the program can be combined with others that reference these symbols. |
| **register** | The assembler recognizes the predefined register symbols shown in Table 7-6. |
| **text** | The value of a `.text` symbol is measured as a number of bytes from the beginning of the `.text` section of the program. When assembler output is linked, `.text` symbols can change in value. Most `.text` symbols are labels in the assembly that define data or instruction locations. At the start of an assembly, the value of the location counter 0 of the `.text` section. |
| **undefined** | When the assembler identifies a new symbol during assembly, the symbol is considered undefined. It becomes defined when it is assigned a value or location. A symbol can subsequently become undefined again if assigned an undefined expression. Undefined operands are not permitted with certain operators. A symbol that remains undefined after assembly is considered an undefined external. |
| **undefined external** | A symbol declared `.globl` but not defined in the current assembly is an undefined external. If you declare such a symbol, use the linker to combine the assembler's output with another routine that defines the undefined reference. |
Table 7-7  Predefined Register Symbols

<table>
<thead>
<tr>
<th>Registers</th>
<th>Symbol</th>
<th>Alias</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>local</td>
<td>r0*</td>
<td>pfp</td>
<td>previous frame pointer</td>
</tr>
<tr>
<td></td>
<td>r1*</td>
<td>sp</td>
<td>stack pointer</td>
</tr>
<tr>
<td></td>
<td>r2*</td>
<td>rip</td>
<td>return instruction pointer</td>
</tr>
<tr>
<td></td>
<td>r3 through r15</td>
<td></td>
<td>general-purpose</td>
</tr>
<tr>
<td>global</td>
<td>g0 through g13</td>
<td></td>
<td>general-purpose</td>
</tr>
<tr>
<td></td>
<td>g14</td>
<td></td>
<td>linkage for bal instruction</td>
</tr>
<tr>
<td></td>
<td>g15*</td>
<td>fp</td>
<td>frame pointer</td>
</tr>
<tr>
<td>floating-point</td>
<td>fp0 through fp3</td>
<td></td>
<td>general-purpose</td>
</tr>
<tr>
<td>special function</td>
<td>sf0 through sf4</td>
<td></td>
<td>registers for architecture-specific functions such as DMA or cache control. See your processor user’s manual.</td>
</tr>
<tr>
<td>processor state</td>
<td>ip</td>
<td></td>
<td>instruction pointer</td>
</tr>
<tr>
<td></td>
<td>ac</td>
<td></td>
<td>arithmetic controls</td>
</tr>
<tr>
<td></td>
<td>pc</td>
<td></td>
<td>process controls</td>
</tr>
<tr>
<td></td>
<td>tc</td>
<td></td>
<td>trace controls</td>
</tr>
</tbody>
</table>

* You must use the aliases, not the symbols, for registers r0, r1, r2, and g15.

Example 7-2 uses local, global, floating-point registers, and the instruction pointer and is valid only for processors with the numerics architecture (i960 SB or KB processors). Users targeting the KA, SA, CA, CF, JA, JF, JD, JN, HA, HD, HT, RD, or RP processor can use the AFP-960 library for emulated floating-point operation, which is described in the *i960 Processor Library Supplement*. In the assembly source, the register names must not be capitalized.
Example 7-3  Example of Register Usage
/* example of fp register usage */
movr 1.0, fp0      # set fp0 = 0f+1.0
movr fp1, r6      # convert real formats
ld 0(g14), r0     # load based on g14
addr 1.0, fp1, g8 # g8:g9 = fp1 + 0f+1.0
st g5, 4(ip)      # store based on ip
 lda (ip), g14     # g14 = value of ip

As shown in the example, the instruction pointer register can be used only to indicate indirection in instructions that allow an IP indirect addressing mode. You cannot use \texttt{ip} as an operand specifier by itself; it is not a general-purpose register. See the Memory-addressing Modes section in this chapter for additional information on memory addressing modes.

The special function registers \texttt{sf0} through \texttt{sf2} are defined in the i960 processor architecture but implemented only on the CA and CF processors. The i960 Hx processor supports special function registers \texttt{sf0} through \texttt{sf4}. For more information about these registers, see your processor manual.

Type Propagation in Expressions

When operands are combined using operators, the resulting expression is assigned a type that depends on the types of the operands and on the operator. For purposes of expression evaluation, the assembler recognizes these types:

- undefined
- absolute
- text
- data
- bss
- undefined external
When the assembler evaluates an expression with operands of different types, the type of the resulting expression is determined by the following rules:

- When one of the operands is undefined, the result is undefined.
- When both operands are absolute, the result is absolute.
- When an absolute is combined with a type that is not absolute (relocatable), the result is the same type as the non-absolute operand.

These rules apply to the following binary operators. At least one operand must be absolute; any other combination is illegal:

+ When one operand is a relocatable .text, .data, or .bss symbol or an undefined external symbol, the result has the postulated type: the other operand must be absolute.

− When the first operand is a relocatable, the result is relocatable.

   When both operands are absolute, the result is absolute.

**Comments**

The assembler recognizes the following as comments:

- Standard comments introduced by the # character.
- C-style comments placed between /* and */ characters.

The # character introduces a comment that extends through the end of the line on which it appears.

The assembler also recognizes C-style comments, introduced with /* and ending with */. C-style comments cannot be nested. The first */ token terminates the comment, regardless of the number of */ tokens preceding it. C-style comments can extend across multiple lines.
Summary of Core Instructions

The core instruction set implements ordinal and integer arithmetic operations along with program and processor control functions that support the architecture. In this manual, the core instruction set is divided into these categories:

- **Data manipulation and processing**: These instructions move data, convert between different data types, and perform basic arithmetic and boolean operations.
- **Program control**: These instructions alter the normal execution sequence based upon specified conditions. These instructions include ordinal and integer comparisons, branching, and procedure call and return.
- **Processor support**: These instructions explicitly or implicitly make use of features of the i960 processor: including fault, trace, and process controls words, IAC messages, and multiprocessor design support.

Data Movement

The data movement instructions transfer integer and ordinal data between memory and the global and local registers (load and store instructions) and between registers (move instructions). The mnemonic opcodes indicate the size and type of data.

Besides moving data, the data movement instructions implicitly convert between different data types. For example, the load integer short instruction (ldis) copies a half-word (16 bits) from memory into a register. The ldis instruction implicitly converts the half word to a full word in the register, and the processor automatically sign-extends the high-order 16 bits.
Load

These instructions copy data from memory to selected registers or register groups:

- `ld`  load
- `ldcb`  load byte ordinal
- `ldos`  load short ordinal
- `ldib`  load byte integer
- `ldis`  load short integer
- `ldl`  load long
- `ldt`  load triple
- `ldq`  load quad
- `lda`  load address

All the load instructions use the MEM instruction format. Except for load address, which stores the memory location address itself in the designated register, the load instructions copy data from the addressed location to a specified register or successive registers.

Byte and short ordinal operands are zero-extended when loaded; byte and short integers are automatically sign-extended. Multi-register operations require appropriate register alignment. Besides moving data, these instructions are used for implicit data type conversions.

Store

These instructions copy data from selected registers or register groups to memory:

- `st`  store
- `stcb`  store byte ordinal
- `stos`  store short ordinal
- `stib`  store byte integer
- `stis`  store short integer
Assembly Language

The store instructions use the MEM instruction format. The store instructions copy data from the specified register or successive registers to the addressed location. The processor reformats short and byte ordinal and integer operands for the smaller memory location. Multi-register operations require appropriate register alignment.

**Move**

The move instructions copy data from a selected register or register group to another register or register group:

- mov : move word
- movl : move long
- movt : move triple
- movq : move quad

To move data in real format between the global or local registers and the floating-point registers, the numerics architecture of the KB and SB processors provides a set of move real instructions. Multi-register operations require appropriate register alignment.

**Select**

These data movement instructions are available on the i960 Jx, Hx, and Rx processors. They select one of two source registers to copy into a destination register, based on the status of the condition code. All are REG format instructions.

- selno : select based on unordered
- selg : select based on greater
- sele : select based on equal
- selge : select based on greater or equal
sell
select based on less
selne
select based on not equal
selle
select based on less or equal
selo
select based on ordered

Ordinal and Integer Arithmetic

Core instructions that perform ordinal, integer, and decimal arithmetic belong to the following categories:

• basic arithmetic
• extended arithmetic
• conditional arithmetic
• remainder and modulo
• shift and rotate

All the instructions in this category use the REG instruction format.

Basic Arithmetic

These instructions perform the basic arithmetic operations: add, subtract, multiply, and divide:

addo
add ordinal
addi
add integer
subo
subtract ordinal
subi
subtract integer
mulo
multiply ordinal
mul
multiply integer
divo
divide ordinal
divi
divide integer

The basic arithmetic operations are carried out on ordinal and integer word operands contained in global or local registers. Use the load and store instructions to move data between memory and the registers.
Extended Arithmetic

The extended arithmetic instructions support operations on single- or dual-word operands:

- `addc`  add ordinal with carry
- `subc`  subtract ordinal with carry
- `emul`  extended multiply
- `ediv`  extended divide

In the add and subtract with carry instructions, the carry bit in the condition code (CC) of the arithmetic controls word (AC) participates in the operation. The integer overflow flag in the AC (used with the integer overflow mask) is set to indicate whether or not an overflow condition resulted from the operation. These two instructions facilitate multiple-precision addition and subtraction in assembly language programs.

The extended multiply (`emul`) instruction multiplies two ordinals in registers and copies the result into an aligned dual-register group. The extended divide (`ediv`) instruction performs the inverse operation, dividing a long ordinal (double-word) by an ordinal (word) resulting in a quotient and remainder (both ordinals) in a dual-register group.

Conditional Arithmetic

The conditional arithmetic instructions are available on the i960 Jx and Hx processors. They combine addition or subtraction with checking the condition code. They add or subtract the two source registers and copy the result into the destination, but only if the status of the condition code is correct for the given instruction. All are REG format instructions.

- `addono`  add ordinal if ordered
- `addog`  add ordinal if greater
- `addoe`  add ordinal if equal
- `addoge`  add ordinal if greater or equal
- `addol`  add ordinal if less
<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>addone</td>
<td>add ordinal if not equal</td>
</tr>
<tr>
<td>addole</td>
<td>add ordinal if less or equal</td>
</tr>
<tr>
<td>addoo</td>
<td>add ordinal if ordered</td>
</tr>
<tr>
<td>addino</td>
<td>add integer if ordered</td>
</tr>
<tr>
<td>addig</td>
<td>add integer if greater</td>
</tr>
<tr>
<td>addie</td>
<td>add integer if equal</td>
</tr>
<tr>
<td>addige</td>
<td>add integer if greater or equal</td>
</tr>
<tr>
<td>addil</td>
<td>add integer if less</td>
</tr>
<tr>
<td>addine</td>
<td>add integer if not equal</td>
</tr>
<tr>
<td>addile</td>
<td>add integer if less or equal</td>
</tr>
<tr>
<td>addio</td>
<td>add integer if ordered</td>
</tr>
<tr>
<td>subono</td>
<td>subtract ordinal if ordered</td>
</tr>
<tr>
<td>subog</td>
<td>subtract ordinal if greater</td>
</tr>
<tr>
<td>suboe</td>
<td>subtract ordinal if equal</td>
</tr>
<tr>
<td>suboge</td>
<td>subtract ordinal if greater or equal</td>
</tr>
<tr>
<td>subol</td>
<td>subtract ordinal if less</td>
</tr>
<tr>
<td>subone</td>
<td>subtract ordinal if not equal</td>
</tr>
<tr>
<td>subole</td>
<td>subtract ordinal if less or equal</td>
</tr>
<tr>
<td>suboo</td>
<td>subtract ordinal if ordered</td>
</tr>
<tr>
<td>subino</td>
<td>subtract integer if ordered</td>
</tr>
<tr>
<td>subig</td>
<td>subtract integer if greater</td>
</tr>
<tr>
<td>subie</td>
<td>subtract integer if equal</td>
</tr>
<tr>
<td>subige</td>
<td>subtract integer if greater or equal</td>
</tr>
<tr>
<td>subil</td>
<td>subtract integer if less</td>
</tr>
</tbody>
</table>
subine  subtract integer if not equal
subile  subtract integer if less or equal
subio   subtract integer if ordered

**Remainder and Modulo**
These arithmetic instructions divide the operands and retain the remainder of the operation, discarding the quotient:

remi    remainder integer
remo    remainder ordinal
modi    modulo integer

In the remainder instructions, the result has the same sign as the dividend. The result of the modulo instruction has the same sign as the divisor.

**Shift and Rotate**
The shift and rotate instructions implicitly perform arithmetic functions by shifting the bits in a register operand:

eshro   extended shift right ordinal (i960 Cx, Jx, and Hx processors only)
shlo    shift left ordinal
shro    shift right ordinal
shli    shift left integer
shri    shift right integer
shrdi   shift right dividing integer
rotate  rotate bits

The shift instructions discard bits shifted out of the high-order or low-order bits of the register. The rotate instruction replaces bits shifted out of the high-order bits of the operand in the vacated low-order bit positions.
The shift right integer instruction does not correctly divide negative operands by powers of two arithmetic, although it does perform a conventional shift operation. To divide negative integer operands correctly, use the shift right dividing integer (shrdi) instruction instead of the shift right integer (shri) instruction.

The extended shift right ordinal instruction (eshro) is the equivalent of an extended divide by a power of 2, which produces no remainder.

**Logical**

These instructions perform the bitwise boolean (logical) functions on word operands in the specified registers. The only unary operation is carried out by the not instruction, which negates the bits in the src operand, represented by A in the list below.

In describing the remaining logical instructions, the letter A represents a bit in the src2 operand and B represents the corresponding bit in the src1 operand.

---

**NOTE.** The binary logic functions process the source operands in reverse order.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>not</td>
<td>not A</td>
</tr>
<tr>
<td>and</td>
<td>A and B</td>
</tr>
<tr>
<td>notand</td>
<td>(not A) and B</td>
</tr>
<tr>
<td>andnot</td>
<td>A and (not B)</td>
</tr>
<tr>
<td>nand</td>
<td>not (A and B)</td>
</tr>
<tr>
<td>or</td>
<td>A or B</td>
</tr>
<tr>
<td>notor</td>
<td>(not A) or B</td>
</tr>
<tr>
<td>ornot</td>
<td>A or (not B)</td>
</tr>
</tbody>
</table>
nor  not (A or B)
xor  not (A = B)
xnor A = B

Tables 7-8 through 7-10 show the operands and results of the binary logical operations. The unary not instruction simply complements bits (clears bits that are set and sets bits cleared to 0) in a bitwise fashion for each of the 32 bits of the src operand.

**Table 7-8  Unary Operation**

<table>
<thead>
<tr>
<th>A</th>
<th>not</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**Table 7-9  Binary Operations**

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>and</th>
<th>notand</th>
<th>andnot</th>
<th>nand</th>
<th>or</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

**Table 7-10  Binary Operations Continued**

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>notor</th>
<th>ornot</th>
<th>nor</th>
<th>xor</th>
<th>xnor</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>
Bit, Bit Field, Byte

The bit and bit field instructions perform operations on a contiguous series of bits within an ordinal word. As with the arithmetic instructions, the bit and bit field instructions operate only on data placed in global or local registers. Use the data movement instructions to transfer data between memory and the registers. The processor also provides two byte operations, \texttt{scanbyte} and \texttt{bswap}.

Bit Operations

These instructions operate on a single specified bit in a global or local register.

\begin{verbatim}
setbit          set bit
clrbit          clear bit
notbit          not bit
chkbit          check bit
alterbit        alter bit
scanbit         scan for bit
spanbit         span over bit
\end{verbatim}

The \texttt{setbit}, \texttt{clrbit}, and \texttt{notbit} instructions set, clear, or complement the specified bit in an ordinal word. The \texttt{chkbit} instruction sets the condition code (CC) in the arithmetic controls word (AC) according to the state of the specified bit. The \texttt{alterbit} instruction changes the state of the bit based on the condition code setting.

The \texttt{scanbit} and \texttt{spanbit} instructions return the bit number of the most-significant set and clear bit in the source operand, respectively.
Bit Field Operations

Two instructions operate on a bit field, specified by the bit position of the least-significant bit in the field and the length of the field:

- `extract` extract bit field
- `modify` modify under mask

The `extract` instruction shifts the specified bit field to the right and fills the vacated high-order positions with zeros. The `modify` instruction copies the specified bit field in one register to another, under control of a mask. This instruction preserves bits corresponding to masked bit positions.

Byte Operations

The `scanbyte` instruction compares two ordinals on a byte-by-byte basis, testing whether or not any two corresponding bytes in the ordinals are equal. The `scanbyte` instruction then sets the condition code (CC) according the outcome: successful (TRUE) or unsuccessful (FALSE).

The `bswap` instruction, available only on i960 Jx, Hx, and Rx processors, reverses the byte order within a 4-byte word. Bytes 0 and 3 are swapped, and bytes 1 and 2 are swapped. This is a REG format instruction.

Comparison

Several types of instructions facilitate the comparison of instruction operands. These instructions often are used for program decision-making and can result in a subsequent call or branch. Compare and conditional-compare instructions, as well as compare-and-increment or compare-and-decrement instructions, are included in the core architecture.

The comparison instructions use REG format and operate on the following types of data:
- ordinal
- integer
- real
This chapter discusses comparison of ordinal and integer data types; the real data types and related operations are discussed in your processor manual.

**Compare and Conditional Compare**

The following instructions compare the specified operands, in global or local registers, and set the condition code (CC) in the arithmetic controls word (AC) according to the results of the test:

- `cmpi` compare integer
- `cmpo` compare ordinal
- `concmpi` conditional-compare integer
- `concmpo` conditional-compare ordinal
- `cmpob` compare ordinal byte
- `cmpib` compare integer byte
- `cmpos` compare ordinal short
- `cmpis` compare integer short

The byte and short versions of this instruction are available only on the i960 Jx and Hx processors.

The `cmpi` and `cmpo` instructions simply test the operands and set the condition code. The `concmpi` and `concmpo` instructions first examine the status bit (bit 2) of the condition code and compare the operands only if the status bit is not set. If the status bit is set, no further action occurs.

These instructions optimize two-sided range comparisons, to test whether a given value lies between two others. A compare instruction (`cmpi` or `cmpo`) checks one side of the range and a conditional-compare instruction (`concmpi` or `concmpo`) checks the other, based upon the result of the first comparison.
Compare and Increment or Decrement

The following compare-and-increment or compare-and-decrement instructions compare two specified source operands and set the condition code based on the result:

- cmpinci: compare and increment integer
- cmpinco: compare and increment ordinal
- cmpdeci: compare and decrement integer
- cmpdeco: compare and decrement ordinal

These instructions either increment or decrement the destination register by 1. The compare-and-increment or compare-and-decrement instructions provide a convenient way to control iterative program loops.

Branch

The branch instructions direct the processor to continue executing a program's instructions at another memory address, sometimes conditionally. To accomplish this end, these instructions modify the current instruction pointer (IP). The new value of the IP can be specified as a displacement applied to the instruction pointer (COBR and CTRL instruction formats), or defined using several memory addressing modes (MEM instruction formats).

The branch instructions provide the following program control functions:
- unconditional branch
- conditional branch
- compare and branch

In addition to these machine instructions, Chapter 8 describes several sets of pseudo-instructions to simplify coding branch instructions.
Unconditional Branch

The following instructions direct the processor to continue executing instructions from a supplied address under any condition:

- \texttt{b} \quad \text{branch}
- \texttt{bx} \quad \text{branch extended}
- \texttt{bal} \quad \text{branch and link}
- \texttt{balx} \quad \text{branch and link extended}

The branch (\texttt{b}) instruction uses the CTRL format, with a limited addressing range, while the branch extended (\texttt{bx}) instruction uses MEM format with a full addressing range and corresponding memory address modes.

Like the branch instructions, the \texttt{bal} and \texttt{balx} instructions use CTRL and MEM formats, respectively. These instructions save the address of the next sequential instruction and branch unconditionally to the specified address.

Typically, the branch-and-link instructions are used to pass control to local program procedures. (Local procedures are procedures that do not require the processor’s call-and-return mechanism.)

Conditional Branch

The following instructions direct the processor to continue executing instructions from a supplied address depending on the status of the condition code (CC) bits in the arithmetic controls (AC) word:

- \texttt{be} \quad \text{branch if equal}
- \texttt{bne} \quad \text{branch if not equal}
- \texttt{bl} \quad \text{branch if less}
- \texttt{ble} \quad \text{branch if less or equal}
- \texttt{bg} \quad \text{branch if greater}
bge  branch if greater or equal
bo   branch if ordered
bno  branch if unordered

These instructions also use the CTRL format and specify the target memory address as a displacement from the current instruction pointer (IP). Use the branch if ordered (bo) and branch if unordered (bno) to compare real number operands.

A set of branch real pseudo-instructions supplement the bo and bno instructions to include comparisons of real numbers. In addition, the branch if true (bt) and branch if false (bf) directives provide convenient mnemonics for branching on specific conditions. See Chapter 8 for more information on the branch pseudo-instructions.

**Compare and Branch**

The ordinal and integer compare-and-branch instructions compare the two source operands, set the condition code (CC), and branch to the specified address depending on the result. These instructions are:

- `cmpobe` compare ordinal and branch if equal
- `cmpobne` compare ordinal and branch if not equal
- `cmpobil` compare ordinal and branch if less
- `cmpoble` compare ordinal and branch if less or equal
- `cmpobg` compare ordinal and branch if greater
- `cmpobge` compare ordinal and branch if greater or equal
- `cmpibo` compare integer and branch if ordered
- `cmpib` compare integer and branch if equal
- `cmpibne` compare integer and branch if not equal
- `cmpibl` compare integer and branch if less
- `cmpible` compare integer and branch if less or equal
cmpibg  compare integer and branch if greater
cmpibge compare integer and branch if greater or equal
cmpibno compare integer and branch if not ordered

Two other compare and branch instructions operate on a single-bit operand in an ordinal word in a global or local register:

bbc  branch on bit clear
bbs  branch on bit set

All compare-and-branch instructions use the COBR instruction format, implying a limited address range. See also the compare-and-jump pseudo-instructions, described in Chapter 8.

**Call and Return**

For programming convenience, i960 processors provide various mechanisms for making procedure calls. The following instructions support the processor's call-and-return mechanism:

call  call to local procedure using 24-bit addressing
callx call to procedure using full 32-bit addressing
calls call to a system procedure
ret  return

Like the branch instructions, the call instruction uses the CTRL format, with a limited addressing range, while the callx instruction uses MEM format with a full addressing range and corresponding memory address modes.

The calls instruction provides a supervisor call capability, deriving the procedure address from the system procedure table, using a specified index number to determine the correct table entry to reference. The table entry determines whether procedures in the table can execute in supervisor mode. Upon return from the called procedure, the processor resumes its previous execution mode.
The assembler provides two pseudo-instructions which are optimized by the linker:

- `callj` stands for a `call`, `bal`, or `calls` instruction
- `calljx` stands for a `callx`, `balx`, or `calls` instruction

With the `callj` and `calljx` pseudo-instructions, you can make symbolic references to a variety of function types without using an explicit call or branch-and-link instruction. The linker chooses the appropriate instruction or instruction sequence for the symbol type and performs call optimization, if possible. For additional information on call optimization, see the i960 Processor Software Utilities User’s Guide.

### Fault

Normally, the processor implicitly generates faults when exceptions occur and handles them automatically through the programmer-defined fault table. The address of the fault table is supplied to the processor at initialization time. You can inhibit certain faults by using the fault controls, or masks.

The following fault-if instructions allow a running program to raise a fault condition explicitly:

- `faulte` fault if equal
- `faultne` fault if not equal
- `faultl` fault if less
- `faultle` fault if less or equal
- `faultg` fault if greater
- `faultge` fault if greater or equal
- `faulto` fault if ordered
- `faultno` fault if unordered

The processor services a fault generated by one of these instructions as if it were generated implicitly, as a result of an exception. See your processor-manual for information on enabling and masking faults.
Chapter 8 explains the fault if true (faultt) and fault if false (faultf) assembler pseudo-instructions that provide a mnemonic method for generating faults based on logic conditions.

**Debug**

Several processor instructions support the processor's on-chip debugging facilities. These facilities include a trace controls word and associated masks, allowing the program to enable or disable specific types of trace functions. The debug instructions are:

- **modtc** modify trace controls
- **mark** mark a breakpoint
- **fmark** force mark a breakpoint

The **modtc** instruction allows a running program to change the bits in the processor's trace controls word. The **mark** and **fmark** instructions generate a breakpoint trace event: the **mark** instruction generates the event if the breakpoint trace mode is enabled by the trace controls word, while the **fmark** instruction generates an unconditional breakpoint event.

See your processor manual for information on the trace mechanism and associated controls.

**Processor Management**

The following instructions read or modify bits in the arithmetic and processor controls words:

- **modac** modify arithmetic controls
- **modpc** modify process controls
- **sysctl** perform system control function on the i960 Cx, Jx or Hx processors
Note that with there are special rules for using a \texttt{modpc} instruction with the i960 Rx architectures. The syntax for using the \texttt{modpc} instruction with any i960 architecture other than Rx is:

\texttt{modpc src, mask, src/dst}

With the i960 Rx architecture, the first and third arguments must be the same. If these arguments are not the same, the assembler generates a warning.

Another instruction that is useful for processor management is the \texttt{flushreg} instruction. \texttt{flushreg} saves all but the current local register set ensuring that the local register save areas contain the same data as the processor's local register sets.

The following processor management instructions are specific to the i960 Jx, Rx, and Hx processors:

\begin{table}[h]
\centering
\caption{Supported Processor Management Instructions}
\begin{tabular}{|l|l|c|c|c|}
\hline
Instruction & Description & 80960Jx & 80960Rx & 80960Hx \\
\hline
\texttt{intdis} & global interrupt disable & Yes & Yes & Yes \\
\texttt{inten} & global interrupt enable & Yes & Yes & Yes \\
\texttt{intctl} & global enable and disable of interrupts & Yes & No & Yes \\
\texttt{icctl} & icache control & Yes & Yes & Yes \\
\texttt{dcctl} & dcache control & Yes & Yes & Yes \\
\texttt{halt} & halt CPU & Yes & No & No \\
\texttt{dcinva} & data cache invalidate by address & No & No & Yes \\
\hline
\end{tabular}
\end{table}

The following test-if instructions allow programs to examine the bits of the condition code, which can then be used to redirect program flow:

\begin{itemize}
\item \texttt{teste}: test if equal
\item \texttt{testne}: test if not equal
\item \texttt{testl}: test if less
\end{itemize}
testle  test if less or equal
etestg  test if greater
etestge test if greater or equal
etesto  test if ordered
etestno test if unordered

**Synchronous (K-series only)**

On K-series processors, the synchronous instructions move data from a register to memory or from one memory location to another.

- **synld**  synchronous load
- **synmov**  synchronous move
- **synmovl** synchronous move long
- **synmovq** synchronous move quad

The `synld` instruction copies a word from a register into memory. The synchronous move instructions transfer data from one location in memory to another.

Normally the processor executes store instruction asynchronously with respect to the memory controller. That is, after placing information on the data bus for storage in memory, the processor assumes that bus control logic carries out the operation and continues with the next instruction. In contrast, the synchronous instructions perform store and move operations synchronously with memory.

When executing any of the synchronous instructions, the processor must wait until that instruction and any other pending memory access instructions are completed before executing the next instruction.

The processor indicates that a synchronous instruction is complete by setting the condition code bit (CC) in the arithmetic controls word (AC). Use these instructions when you must be sure that memory operations are completed before further processing takes place, as in multiprocessor designs. See also the section on atomic instructions below.
Also, the synchronous instructions can be used as a mechanism to avoid interrupts when sending interagent communication (IAC) messages.

Atomic

An atomic access is a processor read-modify-write operation on a 32-bit word of memory. In multiple-processor designs, while one processor performs an atomic access, other processors in the system cannot access the same memory block until the original operation is complete. The atomic instructions are:

- `atadd` atomic add
- `atmod` atomic modify

The `atadd` and `atmod` instructions add or modify the data in a specified memory location and guarantee the integrity of the operation.

Summary of On-chip Numerics Instructions

Floating-point instructions have at least one operand that is a real data type. They include the following functional categories of instructions:

- data movement instructions
- sign copying instructions
- data type conversion instructions
- comparison and classification instructions
- basic arithmetic instructions
- trigonometric functions
- logarithmic, exponential, and scale instructions
- decimal data manipulation instructions

The following sections summarize the instructions in each group.

Data Movement

Several ordinal and integer load and store instructions (`ld/st`, `ldl/stl`, `ldt/stt`, `ldq/stq`) move 4, 8, 12, or 16 bytes of data between memory and local or global registers without regard to data type. The core architecture move instructions (`mov`, `movl`, `movt`, `movq`) can then transfer
the contents of 1 to 4 local or global registers to another non-overlapping group of 1 - 4 local or global registers without changing formats: real values remain real, integer values remain integer, and so on.

Three move real instructions are provided in the numerics architecture:

- **movr**: move real
- **movrl**: move long-real
- **movre**: move extended-real

The **movr** and **movrl** instructions are most often used to transfer real-valued data between global and local registers and floating-point registers when a format change is desired. This technique implicitly converts 32-bit, 64-bit, or 96-bit real data to 80-bit extended-real format and vice versa.

The following procedure converts 32-bit real data to a 64-bit real representation:

1. Move a 32-bit real data word into a floating-point register using the **movr** instruction. This step implicitly converts the real value into an extended-real value.
2. Move the extended-real value from the floating-point register to two global or local registers using the **movrl** instruction. The processor explicitly converts the extended-real number into a 64-bit long-real value in two global or local registers.

To convert implicitly from real and long-real to extended-real data format, use the floating-point registers as operands in arithmetic, trigonometric, logarithmic, and exponential operations.

The **movre** instruction copies extended-real values between a 80-bit floating-point register and a triple global or local register group (96 bits). The instruction does not alter the data type. However, when moving data from a floating-point register to a register group, the **movre** instruction inserts 16 zeros in the high-order bit positions to pad the third data word. When moving the contents of the register group to a floating-point register, this instruction deletes the most significant 16 bits of the word in the third register.
Sign Copying

The numerics architecture provides two sign-copying instructions:

- `cpysre` copy sign extended-real
- `cpyrsre` copy reverse sign extended-real

These instructions enable you to copy the sign of one extended-real value, or its reverse, to another. Both operate exclusively on extended-real data types, and at least one of the values must be in a floating-point register. To copy the signs of real or long-real values, use the `chkbit` and `alterbit` instructions.

Data Type Conversion

To convert between floating-point formats, for example between real and extended-real formats, use the move real instructions described in the Data Movement section. To convert between integer and real number formats, the numerics architecture provides these explicit instructions:

- `cvtir` convert integer to real
- `cvtilr` convert long integer to real
- `cvtri` convert real to integer
- `cvtril` convert real to long integer
- `cvtzri` convert truncated real to integer
- `cvtrzril` convert truncated real to long integer

The `cvtir` and `cvtilr` instructions can change their 32-bit and 64-bit data types to 80-bit extended-real values or 32-bit real values, respectively. The move real instructions can then convert the result to 64-bit long-real format if desired.

The `cvtri` and `cvtril` instructions change 32-bit real or 80-bit extended-real numbers to integers. Hence, to convert a 64-bit long-real value to an integer, first convert it to an extended-real format using the appropriate move real instruction. Then use one of the convert real instructions to transform the extended-real value to the desired integer format.
The `cvtzri` and `cvtril` instructions allow efficient implementation of FORTRAN or C-style truncation semantics. They ignore the rounding mode bits in the arithmetic controls word, and round toward zero always.

**Basic Arithmetic**

The following instructions perform the basic arithmetic operations specified in the IEEE standard:

- `addr` add real
- `addrl` add long-real
- `subr` subtract real
- `subrl` subtract long-real
- `mulr` multiply real
- `mulrl` multiply long-real
- `divr` divide real
- `divrl` divide long-real
- `remr` remainder real
- `remrl` remainder long-real
- `roundr` round real
- `roundrl` round long-real
- `sqrtr` square root real
- `sqrtrl` square root long-real

These instructions correspond to many of the core architecture instructions in the same functional category. However, in the numerics architecture all arithmetic operations require real or long-real data types as operands and result in real numbers.

The results and operands of instructions such as `addr`, `subr`, `mulr`, etc., can be 32-bit real, or 80-bit extended-real values. Similarly, results and operands of the arithmetic long-real instructions, such as `addrl`, `subrl`, and `mulrl`, can be 64-bit long-real, or 80-bit extended-real values.
The add, subtract, multiply, divide, and square root instructions represent relatively standard, straightforward mathematical functions performing the operations their names imply.

The `remr` and `remrl` instructions divide the contents of a register or dual-register group by the value in another register (or pair) and produce the remainder of the quotient; the quotient itself is ignored. For example, if the real number 987.34 is divided by 185.769, the quotient is 5.31488... and the remainder is the fractional portion of the quotient, .31488... These instructions differ from the IEEE standard by the way in which the integer portion of the quotient is determined.

The `roundr` and `roundrl` instructions convert a real or long-real operand to an integer value based on the current rounding mode. The integer result remains in floating-point format. The current rounding mode is determined by the setting of the rounding mode bits in the arithmetic controls word (AC).

For example, the real-valued result 137.85 is rounded to 137.0 if the rounding controls are set to round toward zero. The same number is rounded to 138.0 if the rounding controls are set to round to infinity.

**Decimal**

The decimal instructions operate on 32-bit operands that contain an ASCII-coded decimal digit in the least-significant 8 bits of the data word.

- `dmovt` decimal move and test
- `daddc` decimal add with carry
- `dsubc` decimal subtract with carry

The `dmovt` instruction moves a 32-bit word from one register to another and tests the least-significant byte of the operand to determine if it is a valid ASCII-coded decimal digit (00110000₂ through 00111001₂, corresponding to the decimal digits 0 through 9). For valid digits, the condition code (CC) is set to 000₂; otherwise the condition code is set to 010₂.
The `daddc` and `dsubc` instructions operate on two decimal digits. Bit 1 of the condition code indicates a decimal carry-in or carry-out condition. For example, you can use the decimal instructions iteratively to validate ASCII digit strings and to add or subtract ASCII-coded decimal values.

Note that as of CTOOLS release 5.1 and later, the assembler no longer accepts decimal instructions when assembling for a KA or an SA target, since decimal instructions are not supported by those processors.

**Comparison and Classification**

To compare and classify floating-point values, use the numerics instructions:

- `cmpr` compare real
- `cmprl` compare long-real
- `cmpor` compare ordered real
- `cmporl` compare ordered long-real
- `classr` classify real
- `classrl` classify long-real

The `cmpr` and `cmprl` instructions compare the contents of two registers and set the condition code bits (CC) in the arithmetic controls word (AC) to indicate the results of the comparison. For floating-point operands, when at least one comparand is a NaNs, the condition code indicates unordered.

The `cmpor` and `cmporl` instructions set the invalid-operation flag for an unordered condition.

Use the core-architecture branch-ordered (bo) and branch-unordered (bno) instructions to test the floating-point comparison results, with conditional branching if an ordered or unordered condition is detected.

The `classr` and `classrl` instructions determine the class of a real or long-real operand as zero, denormalized finite, normalized finite, infinite, SNaN, or QNaN. The AC arithmetic status bits indicate the result.
Trigonometric Functions

For the common trigonometric functions, use the numerics instructions:

- sinr  sine real
- sinrl sine long-real
- cosr  cosine real
- cosrl cosine long-real
- tanr  tangent real
- tanrl tangent long-real
- atanr arctangent real
- atanrl arctangent long-real

All the trigonometric functions require real or long-real operands and yield floating-point results. The values of angles must be given in radians.

The results and operands of instructions such as sinr, cosr, and tanr can be 32-bit real or 80-bit extended-real values. Similarly, results and operands of the trigonometric long-real instructions, such as sinrl, cosrl, and tanrl, can be in 64-bit long-real or 80-bit extended-real format.

The atanr and atanrl instructions return a result in radians. As well as supplying the inverse tangent of the argument, these instructions facilitate conversion from rectangular to polar coordinates.

If the operands of trigonometric functions are computed using pi, then the full 66-bit representation for pi given in your processor-specific manual must be used. Truncated values are permissible when accuracy is not crucial.
Logarithmic, Exponential, and Scale

For logarithmic, exponential, and scale functions, use the numerics instructions:

- `logbnr`  log binary real
- `logbnrl` log binary long-real
- `logr` log real
- `logrl` log long-real
- `logepr` log epsilon real
- `logeprl` log epsilon long-real
- `expr` exponent real
- `exprl` exponent long-real
- `scaler` scale real
- `scalerl` scale long-real

All these functions require real or long-real operands and yield floating-point results.

The results and operands of instructions such as `logr`, `expr`, and `scaler` can be 32-bit real or 80-bit extended-real format. Similarly, results and operands of the trigonometric long-real instructions, such as `logrl`, `exprl`, and `scalerl` can be in 64-bit long-real or 80-bit extended-real format.

The `logbnr` and `logbnrl` instructions compute the logarithm to the base 2 of the source operand and retain only the integer component. The result is an integer that is the binary log of the given number. For instance, $\log_2 3249 = 11.65532...$, but the binary log function returns the value 11 (decimal) in floating-point format. The `logbnr` and `logbnrl` instructions determine the order of magnitude of a specified number.
The `logr` and `logrl` instructions compute the logarithm to the base 2 of one source operand (`src1`) and scale the result by a second operand (`src2`), to obtain the result (`dst`):

\[ \text{dst} = \text{src1} \times \log_2 \text{src2} \]

By carefully specifying the `src2` operand, logarithms to any base can be computed using these instructions. For instance, by specifying a scale factor of `src1 = .30102...`, the logarithm base 10 (common log) is obtained.

The `logepr` and `logeprl` instructions compute the logarithm to the base 2 of 1.0 plus the `src1` operand and scale (`src2` operand) the result to obtain the result (`dst`):

\[ \text{dst} = \text{src2} \times \log_2 (1.0 + \text{src1}) \]

The `src1` operand is restricted to values near zero which yields maximum accuracy for `1.0 + src1` near unity (i.e., the `src1` operand is close to zero). This condition, for instance, is commonly encountered when computing compound interest. By carefully choosing the `src2` operand, logarithms to any base can be computed.

The `expr` and `exprl` instructions compute the value:

\[ \text{dst} = 2^{\text{src}} - 1 \]

The `src` must be in the range -0.5 to +0.5. The `scale` and `scalerl` instructions multiply the `src2` operand by 2 to an integer power, denoted by the `src1` operand, for the result (`dst`):

\[ \text{dst} = \text{src2} \times 2^{\text{src1}} \]

The exponent and scale instructions can be used together to create an algorithm for computing the value of 2 to any power by noting that:

\[ 2^Y = 2^{(X + I)} = 2^I \times [(2^X - 1) + 1] \]

The `Y` is an arbitrary exponent; `I` and `X` represent the integer and fractional portions of the exponent, respectively.
This chapter describes the pseudo-instructions (pseudo-ops) recognized by the assembler.

Pseudo-instructions appear in the assembly file like valid machine instructions. In actuality, the assembler substitutes one or more machine-level instructions for them. For example, when you enter the optimized load constant or `ldconst`, the assembler selects the fastest instruction available to place the specified value in the designated register. This instruction can be a move, add, subtract, shift, or load-address, depending on the given value.

For convenience, the assembler provides pseudo-instructions that are synonyms for certain branch, fault, load, and compare-and-branch instructions, as described in the following sections. These pseudo-instructions are functions of the assembler and not of any particular processor implementation. In general, you can use them in any assembly language source file. Any implementation-dependent differences are noted.

Syntax

Pseudo-instructions use the same syntax for operands as machine instructions.

The operand names describe the function of the operands (e.g., `src`, `dst`, `targ`).
Branch Pseudo-instructions

The assembler recognizes the pseudo-instructions \texttt{bt} (branch if true) and \texttt{bf} (branch if false) as synonyms for the instructions \texttt{bo} (branch if ordered) and \texttt{bno} (branch if not ordered), respectively.

For convenience in checking the results of real number (floating-point) comparisons, several branch pseudo-instruction are available. Table 8-1 lists these pseudo-instructions with the equivalent instructions.

<table>
<thead>
<tr>
<th>Directive</th>
<th>Operation</th>
<th>Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td>bre</td>
<td>branch real if equal</td>
<td>be</td>
</tr>
<tr>
<td>brg</td>
<td>branch real if greater</td>
<td>bg</td>
</tr>
<tr>
<td>brge</td>
<td>branch real if greater or equal</td>
<td>bge</td>
</tr>
<tr>
<td>brl</td>
<td>branch real if less</td>
<td>bl</td>
</tr>
<tr>
<td>brle</td>
<td>branch real if less or equal</td>
<td>ble</td>
</tr>
<tr>
<td>brlg</td>
<td>branch real if less or greater</td>
<td>bne</td>
</tr>
<tr>
<td>bro</td>
<td>branch real if ordered</td>
<td>bo</td>
</tr>
<tr>
<td>bru</td>
<td>branch real if unordered</td>
<td>bno</td>
</tr>
<tr>
<td>brue</td>
<td>branch real if unordered equal</td>
<td>be,bno</td>
</tr>
<tr>
<td>brug</td>
<td>branch real if unordered greater</td>
<td>bg,bno</td>
</tr>
<tr>
<td>bruge</td>
<td>branch real if unordered greater or equal</td>
<td>bge,bno</td>
</tr>
<tr>
<td>brul</td>
<td>branch real if unordered less</td>
<td>bl,bno</td>
</tr>
<tr>
<td>brule</td>
<td>branch real if unordered less or equal</td>
<td>ble,bno</td>
</tr>
<tr>
<td>brulg</td>
<td>branch real if unordered less or greater</td>
<td>bne,bno</td>
</tr>
</tbody>
</table>

Migration-enabling Pseudo-instructions

Release 6.0 provides a number of pseudo-instructions to ease migration between processors. These pseudo-ops provide an architecture-independent method for performing some of the more common low-level
processing operations. Using these pseudo-ops should reduce the number of changes required when moving assembly code from one i960 processor to another. Table 8-2 lists all of the new pseudo-instructions supported by the CTOOLS assembler.

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>atomic_add</td>
<td>Atomic add</td>
</tr>
<tr>
<td>atomic_modify</td>
<td>Atomic modify</td>
</tr>
<tr>
<td>bkpt_request</td>
<td>Request breakpoint resources</td>
</tr>
<tr>
<td>cc_read</td>
<td>Read condition code</td>
</tr>
<tr>
<td>cc_scanbit</td>
<td>Scan for bit, modifying condition code</td>
</tr>
<tr>
<td>dc_disable</td>
<td>Disable data cache</td>
</tr>
<tr>
<td>dc_enable</td>
<td>Enable data cache</td>
</tr>
<tr>
<td>dc_invalidate</td>
<td>Invalidate data cache</td>
</tr>
<tr>
<td>em_read</td>
<td>Read execution mode</td>
</tr>
<tr>
<td>ic_disable</td>
<td>Disable instruction cache</td>
</tr>
<tr>
<td>ic_enable</td>
<td>Enable instruction cache</td>
</tr>
<tr>
<td>ic_invalidate</td>
<td>Invalidate instruction cache</td>
</tr>
<tr>
<td>ic_load_lock</td>
<td>Load and lock instruction cache</td>
</tr>
<tr>
<td>insn_trace_mode_read</td>
<td>Read instruction trace mode</td>
</tr>
<tr>
<td>insn_trace_mode_set</td>
<td>Set instruction trace mode</td>
</tr>
<tr>
<td>interrupt_state</td>
<td>Read interrupt state</td>
</tr>
<tr>
<td>ip_read</td>
<td>Read instruction pointer</td>
</tr>
<tr>
<td>pri_read</td>
<td>Read execution priority</td>
</tr>
<tr>
<td>sw_reinit</td>
<td>Reinitialize processor</td>
</tr>
<tr>
<td>trace_enable_set</td>
<td>Set trace enable bit</td>
</tr>
</tbody>
</table>
Conditional Faults Pseudo-instructions

The assembler also has equivalent pseudo-instructions that help with conditional faults. The assembler recognizes `faultt` (fault true) and `faultf` (fault false) as synonyms for the instructions `faulto` and `faultno`. These pseudo-instructions have the same syntax as the machine instructions.

Load Pseudo-instructions

The `ldconst` pseudo-instruction automatically optimizes loading of integer and ordinal immediate constant values. Immediate values that cannot be expressed as literals must be explicitly loaded into a register before they can be used as operands for machine instructions. For integer and ordinal operands, loading can be done using the `ldconst` directive. The `ldconst` directive generates different instructions for several different immediate values, based on architecture performance concern. For a list of `ldconst` substitutions, see the Example section of the alphabetical reference entry for `ldconst` later in this chapter.

Call Pseudo-instructions

The `callj` and `calljx` pseudo instructions let you assemble a call instruction, allowing the linker to perform call optimization, when possible. The linker transforms call pseudo-instructions into the appropriate instruction at link time, depending on the type (default, leaf, or system) of the called procedure. See page 8-12 for more information.

Compare-and-jump Pseudo-instructions

For compare-and-branch instructions, the assembler provides a convenient, symbolic way to specify the operation by using a set of compare-and-jump pseudo-instructions.
In the compare (ordinal or integer) and branch-on-condition instructions (such as the `cmpobe` instruction), the branch target must be fewer than $2^{12}$ bytes from the instruction pointer (IP). As an alternative, you can use the compare-and-jump pseudo-instructions provided by the assembler. These pseudo-instructions generate a compare-and-branch (e.g., `cmpobe`) instruction if the target is fewer than $2^{12}$ bytes away, or separate compare and branch instructions otherwise.

Form the compare-and-jump pseudo-instructions by substituting a `j` for the `b` in the corresponding instruction's mnemonic. For example, the instruction `be` becomes pseudo-instruction `je; cmpobe becomes `cmpoje`. As another example, when you used the pseudo-instruction:

```
cmpl je r5, r6, target
```

the assembler generates:

```
compibe r5, r6, target
```

if the label is within $2^{12}$ bytes, or:

```
compi r5, r6
be target
```

otherwise.

**NOTE.** These pseudo-instructions never generate a branch-extended instruction. If you cannot guarantee that the branch address is fewer than $2^{23}$ bytes away from the instruction pointer, you must use the equivalent extended instruction sequence.
The compare-and-jump pseudo-instructions appear in Table 8-3. Each pseudo-instruction is paired with the operation it performs.

### Table 8-3 Compare-and-jump Pseudo-instructions

<table>
<thead>
<tr>
<th>Pseudo-instruction</th>
<th>Full Function Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>cmpije</td>
<td>compare integer and jump if equal</td>
</tr>
<tr>
<td>cmpijg</td>
<td>compare integer and jump if greater</td>
</tr>
<tr>
<td>cmpijge</td>
<td>compare integer and jump if greater or equal</td>
</tr>
<tr>
<td>cmpijl</td>
<td>compare integer and jump if less</td>
</tr>
<tr>
<td>cmpijle</td>
<td>compare integer and jump if less or equal</td>
</tr>
<tr>
<td>cmpijne</td>
<td>compare integer and jump if not equal</td>
</tr>
<tr>
<td>cmpoje</td>
<td>compare ordinal and jump if equal</td>
</tr>
<tr>
<td>cmpojg</td>
<td>compare ordinal and jump if greater</td>
</tr>
<tr>
<td>cmpojge</td>
<td>compare ordinal and jump if greater or equal</td>
</tr>
<tr>
<td>cmpojl</td>
<td>compare ordinal and jump if less</td>
</tr>
<tr>
<td>cmpojle</td>
<td>compare ordinal and jump if less or equal</td>
</tr>
<tr>
<td>cmpojne</td>
<td>compare ordinal and jump if less not equal</td>
</tr>
</tbody>
</table>

Two pseudo-instructions never branch:

- `cmpijno` compare integer and jump if not ordered.
- `cmpojno` compare ordinal jump if not ordered. The equivalent instruction is `cmpibo`.

Two pseudo-instructions always branch:

- `cmpijo` compare integer and jump if ordered.
- `cmipojo` compare ordinal and jump if ordered. The equivalent instruction is `cmpibo`.

Ordered relationships apply only to real numbers on i960 processors with on-chip floating-point capability. The branch instructions for ordered and unordered numbers are consistent ways to provide null operations (no-ops).
Pseudo-instructions Reference

This section describes the pseudo-instructions in alphabetical order.

The syntax descriptions use the placeholder \texttt{targ} for any operand that is an expression representing a memory address. The assembler treats a \texttt{targ} operand as a signed displacement value representing an IP-relative address, as follows:

<table>
<thead>
<tr>
<th>Format</th>
<th>Displacement in Words</th>
</tr>
</thead>
<tbody>
<tr>
<td>COBR</td>
<td>-2^{10} through 2^{10}-1</td>
</tr>
<tr>
<td>CTRL</td>
<td>-2^{21} through 2^{21}-1</td>
</tr>
</tbody>
</table>

atomic\_add

\textit{Atomic Add}

Syntax

\begin{verbatim}
atomic\_add addr, src, dst
reg     reg/lit reg
\end{verbatim}

Discussion

Adds \textit{src} value (full word) to value in the memory location specified with \textit{addr} operand. Initial value from memory is stored in \textit{dst}. Memory read and write are done atomically (i.e., other bus masters must be prevented from accessing the word of memory containing the word specified by \textit{src/dst} operand until operation completes). Memory location in \textit{addr} is the word’s first byte (LSB) address. Address is automatically aligned to a word boundary.

Expansion: \quad Processor \quad Output
\begin{verbatim}
Cx, Jx, Hx atadd addr, src, dst
\end{verbatim}
atomic_modify
Atomic Modify

Syntax

atomic_modify  addr,  mask,  src/dst
              reg    reg/lit    reg

Discussion
Copies the selected bits of src/dst value into memory location specified in addr. Bits set in mask operand select bits to be modified in memory. Initial value from memory is stored in src/dst. Memory read and write are done atomically (i.e., other bus masters must be prevented from accessing the word of memory containing the word specified with the src/dst operand until operation completes). Memory location in addr is the modified word’s first byte (LSB) address. Address is automatically aligned to a word boundry.

Expansion:  Processor        Output
            Cx, Jx, Hx       atmod addr, mask, src/dst
**bkpt_request**

Request Breakpoint Resources

**Syntax**

```
bkpt_request     dst
    reg
```

**Discussion**

Acquires breakpoint resource information. *dst* is set to indicate the available resources. The format of the breakpoint resources status word is listed in Table 8-4.

As a side effect, this pseudo-instruction may modify the condition code on some microprocessors.

**Expansion:**

<table>
<thead>
<tr>
<th>Processor</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jx, Hx</td>
<td>ldconst 0x600,<em>dst</em></td>
</tr>
<tr>
<td></td>
<td>sysctl <em>dst</em>,0,<em>dst</em></td>
</tr>
</tbody>
</table>
Table 8-4. Breakpoint Resource Status Word Bits

<table>
<thead>
<tr>
<th>Bits</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>reserved</td>
</tr>
<tr>
<td>7:4</td>
<td># of available data breakpoints</td>
</tr>
<tr>
<td>3:0</td>
<td># of available instruction breakpoints</td>
</tr>
</tbody>
</table>

**bt, bf**

*Branch if false or branch if true*

bt  
branch if true

bf  
branch if false

**Syntax**

\[
\text{b* target disp}
\]

**Discussion**

Both the `bt` (branch if true) and `bf` (branch if false) directives check the condition code and branch to the location specified by `target` based upon the result of the test.

The assembler recognizes the following correspondence:

<table>
<thead>
<tr>
<th>Directive</th>
<th>Instruction</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>bt</code> (branch if true)</td>
<td><code>bo</code> (branch if ordered)</td>
</tr>
<tr>
<td><code>bf</code> (branch if false)</td>
<td><code>bno</code> (branch if unordered)</td>
</tr>
</tbody>
</table>

The syntax for the two directives is the same as the syntax for the corresponding machine instructions.
### Pseudo-instructions

<table>
<thead>
<tr>
<th>Expansion:</th>
<th>Condition</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>True</td>
<td>bt targ</td>
</tr>
<tr>
<td></td>
<td>False</td>
<td>bf targ</td>
</tr>
</tbody>
</table>

### Example

The assembler changes the pseudo-instruction below to the instruction `bo` process:

```plaintext
bt  process
```

### br<cc>

*Branch on the result of a floating-point comparison*

- `bre`: branch real if equal
- `brg`: branch real if greater
- `brge`: branch real if greater or equal
- `brl`: branch real if less
- `brle`: branch real if less or equal
- `brlg`: branch real if less or greater
- `bro`: branch real if ordered
- `bru`: branch real if unordered
- `brue`: branch real if unordered equal
- `brug`: branch real if unordered greater
- `bruge`: branch real if unordered greater or equal
- `brul`: branch real if unordered less
- `brule`: branch real if unordered less or equal
- `brulg`: branch real if unordered less or greater
Syntax

\texttt{br^* \ targ}
\begin{verbatim}
  disp
\end{verbatim}

Discussion

The branch real directives check the results of floating-point comparisons and branch to the location specified by \texttt{targ} based upon the result of the test. These instructions generate the appropriate compare instructions for unordered cases.

Table 8-1 shows the correspondences between pseudo-instructions and machine instructions.

Use the same syntax for pseudo-instructions you do for the corresponding machine instructions.

Example

The assembler changes the pseudo-instruction below to the instruction \texttt{bno}:
\begin{verbatim}
process:
  bru  process
\end{verbatim}

\textbf{callj, calljx}

\textit{Optimizable linker calls}

Syntax

\begin{verbatim}
  callj \ targ
  disp

  calljx \ targ
  mem
\end{verbatim}
Discussion

The `callj` and `calljx` pseudo-instructions assemble a `call` or `callx` instruction, respectively, and a relocation entry instructing the linker to perform call optimization, when possible. The linker can also be instructed to ignore call optimization. See the utilities user’s guide for more information about linker controls.

When the referenced procedure, represented by `targ`, is a `.leafproc`, the linker replaces the pseudo-instruction with a branch-and-link (`bal` or `balx`) instruction. When the target is a `.sysproc`, the linker replaces the pseudo-instruction with a `calls` instruction.

For example, inserting a `calljx` instruction while using the `-AJD` setting might produce the following linker output depending upon whether the target is a default call, leaf procedure, or system call:

<table>
<thead>
<tr>
<th>Expansion:</th>
<th>Call Type</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Default Call</td>
<td><code>callx _target</code></td>
<td></td>
</tr>
<tr>
<td>Leaf Procedure</td>
<td><code>balx _target,g14</code></td>
<td></td>
</tr>
<tr>
<td>System Call</td>
<td><code>lda _sysprocIndex,g13</code></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td><code>calls (g13)</code></td>
</tr>
</tbody>
</table>

Since `callj` and `calljx` are optimized at link time, examination of the object module generated by the assembler with the disassembler (dumper) displays the assembled instruction as a `call` instruction.

The assembler optimizes `callj` or `calljx` to `bal` or `balx`, respectively, when the referenced procedure is a C language static function.

`callj` can be optimized during assembly when the target of the `callj` is in the same object module and section as the call site.

Example

This sample optimizes a call for procedure `_subx`.

```assembly
callj _subx
```
Changes to the calljx Pseudo-instruction with the i960 Rx Architecture

When used with the -ARD or -ARP option, calljx uses the syntax:

```
calljx _target, tmpreg
```

where `tmpreg` is a local or global register. This change results in the following sequences in the linker:

<table>
<thead>
<tr>
<th>Expansion:</th>
<th>Call Type</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Default Call</td>
<td>lda _target,tmpreg, callx (tmpreg)</td>
<td></td>
</tr>
<tr>
<td>Leaf Procedure</td>
<td>lda _target,tmpreg, balx (tmpreg),g14</td>
<td></td>
</tr>
<tr>
<td>System Call</td>
<td>lda _sysprocIndex,g13, calls (g13)</td>
<td></td>
</tr>
</tbody>
</table>

Notice that with the 80960Rx calljx format all three call types result in a three-word instruction sequence, whereas the previous calljx format requires only two words.

Related Topics

```
bal .leafproc
balx .sysproc
```
**cc_read**

*Read Condition Code*

**Syntax**

```
cc_read  dst
    reg
```

**Discussion**

Copies the current value of the condition code into `dst[2:0]` and zeroes into `dst[31:3]`.

**Expansion:**

<table>
<thead>
<tr>
<th>Processor</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cx</td>
<td>modac 0,0,dst</td>
</tr>
<tr>
<td></td>
<td>and dst,0x7,dst</td>
</tr>
<tr>
<td>Jx, Hx</td>
<td>selg 0,1,dst</td>
</tr>
<tr>
<td></td>
<td>addoe 2,dst,dst</td>
</tr>
<tr>
<td></td>
<td>addol 4,dst,dst</td>
</tr>
</tbody>
</table>
cc_scanbit
Scan For Bit, Modifying Condition Code

Syntax
cc_scanbit src1, dst
reg/lit reg

Discussion
Searches src1 for a set bit (1 bit). If a set bit is found, the bit number of the most significant set bit is stored in the dst and the condition code is set to 010₂. If src1 value is zero, all 1’s are stored in dst and condition code is set to 000₂.

Expansion: Processor Output
Cx, Jx, Hx scanbit src1,dst

cmp*<cc>
Branch to specified target

cmpije compare integer and jump if equal
cMPIJG compare integer and jump if greater
cmpijge compare integer and jump if greater or equal
cmpijle compare integer and jump if less or equal
cmpijne compare integer and jump if not equal
**Pseudo-instructions**

- **cmpijno**: compare integer and jump if not ordered
- **cmpijo**: compare integer and jump if ordered
- **cmpoje**: compare ordinal and jump if equal
- **cmpojg**: compare ordinal and jump if greater
- **cmpojge**: compare ordinal and jump if greater or equal
- **cmpojl**: compare ordinal and jump if less
- **cmpojle**: compare ordinal and jump if less or equal
- **cmpojne**: compare ordinal and jump if less not equal

**Syntax**

- **cmpij**
  - src1, src2, targ
  - reg/lit reg disp

- **cmpoj**
  - src1, src2, targ
  - reg/lit reg disp

**Discussion**

Both the integer and ordinal compare-and-jump directives check the results of a comparison of the contents of the source operands and branch to the location specified by **targ** based upon the resulting condition code (CC). Shown below are the instructions assembled as a result of each of these directives. The assembler recognizes the following correspondences:
Table 8-7  Compare and Jump Substitutions

<table>
<thead>
<tr>
<th>Directive</th>
<th>When Target is &lt; (2^{12}) Bytes Away</th>
<th>When Target is (\geq 2^{12}) Bytes Away</th>
</tr>
</thead>
<tbody>
<tr>
<td>cmpije</td>
<td>cmpibe</td>
<td>cmpi + be</td>
</tr>
<tr>
<td>cmpijg</td>
<td>cmpibg</td>
<td>cmpi + bg</td>
</tr>
<tr>
<td>cmpijge</td>
<td>cmpibge</td>
<td>cmpi + bge</td>
</tr>
<tr>
<td>cmpijl</td>
<td>cmpibl</td>
<td>cmpi + bl</td>
</tr>
<tr>
<td>cmpijle</td>
<td>cmpible</td>
<td>cmpi + ble</td>
</tr>
<tr>
<td>cmpoje</td>
<td>cmpobe</td>
<td>cmpo + be</td>
</tr>
<tr>
<td>cmpojg</td>
<td>cmpobg</td>
<td>cmpo + bg</td>
</tr>
<tr>
<td>cmpojge</td>
<td>cmpobge</td>
<td>cmpo + bge</td>
</tr>
<tr>
<td>cmpojl</td>
<td>cmpobl</td>
<td>cmpo + bl</td>
</tr>
<tr>
<td>cmpojle</td>
<td>cmpoble</td>
<td>cmpo + ble</td>
</tr>
</tbody>
</table>

As Table 8-7 shows, the assembler only generates a compare integer or compare ordinal followed by a branch instruction when the destination is \(2^{12}\) bytes or more away.

Two pseudo-instructions never branch:

- cmpijno: compare integer and jump if not ordered.
- cmpojno: compare ordinal and jump if not ordered. The equivalent instruction is cmpibno.

Two pseudo-instructions always branch:

- cmpijo: compare integer and jump if ordered.
- cmpojo: compare ordinal and jump if ordered. The equivalent instruction is cmpibo.

Ordered relationships apply only to real numbers on i960 processors with on-chip floating-point capability. The branch instructions for ordered and unordered numbers are consistent ways to provide null operations (no-ops), when not used with floating-point values.
The syntax for these directives is the same as the syntax for the corresponding machine instructions in the core architecture.

**Example**

This sample pseudo-instruction uses compare and branch
```assembly
cmpi je r4, g4, process
```
During assembly, the pseudo-instruction becomes the following:
```assembly
cmpi r4, g4
be process
```

---

**dc_disable**

*Disable Data Cache*

**Syntax**

```assembly
dc_disable dst reg
```

**Discussion**

Disables use of the data cache. The data cache status is returned in the *dst* field. The format of the data cache status word is listed in Table 8-8. For Cx processors, *dst* is neither read nor set (i.e., no data cache status is returned). Since the CA processor has no data cache, this operation has no effect on that processor.

**Expansion:**  
Processor:  
<table>
<thead>
<tr>
<th>Expansion:</th>
<th>Processor</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cx</td>
<td></td>
<td>setbit 30, sf2, sf2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>mov g0, g0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>mov g0, g0</td>
</tr>
<tr>
<td>Jx, Hx</td>
<td></td>
<td>dcctl 0, 0, fp</td>
</tr>
<tr>
<td></td>
<td></td>
<td>dcctl 4, 0, dst</td>
</tr>
</tbody>
</table>
Table 8-8  Data Cache Status Word Bits

<table>
<thead>
<tr>
<th>Bits</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>reserved</td>
</tr>
<tr>
<td>27:16</td>
<td># of ways-1</td>
</tr>
<tr>
<td>15:12</td>
<td>$\log_2$(# of sets)</td>
</tr>
<tr>
<td>11:8</td>
<td>$\log_2$(atoms/line)</td>
</tr>
<tr>
<td>7:4</td>
<td>$\log_2$(bytes/atom)</td>
</tr>
<tr>
<td>3:1</td>
<td>reserved</td>
</tr>
<tr>
<td>0</td>
<td>1 = data cache enabled</td>
</tr>
<tr>
<td></td>
<td>0 = data cache disabled</td>
</tr>
</tbody>
</table>

**dc_enable**

*Enable Data Cache*

**Syntax**

```
dc_enable dst reg
```

**Discussion**

Enables use of the data cache. The data cache status is returned in the `dst` field. The format of the data cache status word is listed in Table 8-8. For Cx processors, `dst` is neither read nor set (i.e., no data cache status is returned). Since the CA processor has no data cache, this operation has no effect on that processor.

**Expansion:**

<table>
<thead>
<tr>
<th>Processor</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cx</td>
<td>clrbit 30, sf2, sf2</td>
</tr>
<tr>
<td>Jx, Hx</td>
<td>dcctl 1, 0, fp</td>
</tr>
<tr>
<td></td>
<td>dcctl 4, 0, dst</td>
</tr>
</tbody>
</table>
dc_invalidate

Invalidate Data Cache

Syntax

dc_invalidate  dst
              reg

Discussion

Invalidates the data cache. The data cache status is returned in the dst field. The format of the data cache status word is listed in Table 8-8. For Cx processors, dst is neither read nor set (i.e., no data cache status is returned). Since the CA processor has no data cache, this operation has no effect on that processor.

Expansion:         Processor   Output

Cx                setbit 31,sf2,sf2
                 mov    g0,g0
                 mov    g0,g0

Jx, Hx            dcctl  2,0,fp
                 dcctl  4,0,dst
em_read

Read Execution Mode

Syntax

em_read dst reg

Discussion

If the processor is currently in user mode, sets dst to 0. If the processor is currently in supervisor mode, sets dst to 1.

Expansion: Processor Output

Expansion:  | Processor  | Output
------------|------------|--------
Cx, Jx, Hx  | modpc dst, 0, dst |
            | shro 1, dst, dst |
            | and  0x1, dst, dst |
**faultf, faultt**

*Fault if false or fault if true*

**Syntax**

fault*

**Discussion**

The faultt (fault if true) and faultf (fault if false) directives raise a fault condition based upon a test of the condition code.

The assembler recognizes the following correspondence:

<table>
<thead>
<tr>
<th>Expansion</th>
<th>Condition</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>True</td>
<td>faulto</td>
<td></td>
</tr>
<tr>
<td>False</td>
<td>faultno</td>
<td></td>
</tr>
</tbody>
</table>

The syntax for the two directives is the same as the syntax for the corresponding machine instructions in the core architecture.

**Example**

The following pseudo-instruction becomes faultnof during assembly:

faultf
ic_disable

*Disable Instruction Cache*

**Syntax**

```
ic_disable dst reg
```

**Discussion**

Disables use of the instruction cache. The instruction cache status is returned in the `dst` field. The format of the instruction cache status word is listed in Table 8-9.

**Expansion:** Processor | Output
---|---
Cx | ldconst 0x0201, dst; sysctl dst, 0, 0; ldconst 0x11230, dst
Jx, Hx | icctl 0, 0, fp; icctl 4, 0, dst

**Table 8-9 Instruction Cache Status Word Bits**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>reserved</td>
</tr>
<tr>
<td>27:16</td>
<td># of ways-1</td>
</tr>
<tr>
<td>15:12</td>
<td>(\log_2(#\ \text{of sets}))</td>
</tr>
<tr>
<td>11:8</td>
<td>(\log_2(\text{atoms/line}))</td>
</tr>
<tr>
<td>7:4</td>
<td>(\log_2(\text{bytes/atom}))</td>
</tr>
<tr>
<td>3:1</td>
<td>reserved</td>
</tr>
<tr>
<td>0</td>
<td>1 = instruction cache enabled</td>
</tr>
<tr>
<td></td>
<td>0 = instruction cache disabled</td>
</tr>
</tbody>
</table>


ic_enable
Enable Instruction Cache

Syntax
ic_enable dst reg

Discussion
Enables use of the instruction cache. The instruction cache status is returned in the dst field. The format of the instruction cache status word is listed in Table 8-9.

Expansion: Processor  Output
Cx          ldconst 0x0200, dst
            sysctl  dst,0,0
            ldconst 0x11231, dst
Jx, Hx      icctl 1,0,fp
            icctl 4,0,dst
ic_invalidate

Invalidate Instruction Cache

Syntax

```plaintext
ic_invalidate dst reg
```

Discussion

Invalidates the instruction cache. The instruction cache status is returned in the `dst` field. Bit zero of `dst` is always set to 1 for Cx processors, even if the instruction cache is disabled. The format of the instruction cache status word is listed in Table 8-9.

<table>
<thead>
<tr>
<th>Expansion:</th>
<th>Processor</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cx</td>
<td></td>
<td><code>ldconst 0x0100, dst</code></td>
</tr>
<tr>
<td></td>
<td></td>
<td><code>sysctl dst, 0, 0</code></td>
</tr>
<tr>
<td></td>
<td></td>
<td><code>ldconst 0x11231, dst</code></td>
</tr>
<tr>
<td>Jx, Hx</td>
<td></td>
<td><code>icctl 2, 0, fp</code></td>
</tr>
<tr>
<td></td>
<td></td>
<td><code>icctl 4, 0, dst</code></td>
</tr>
</tbody>
</table>
ic_load_lock
Load and Lock
Instruction Cache

Syntax

\[
ic\_load\_lock \quad addr, \quad src/dst \\
\quad reg \quad reg
\]

Discussion
Loads src/dst blocks into the instruction cache from addr. Locks the affected region of the instruction cache.

Expansion: Processor Output

Jx, Hx icctl 3, addr, src/dst

insn_trace_mode_read
Read Instruction Trace Mode

Syntax

\[
insn\_trace\_mode\_read \quad dst \\
\quad reg
\]

Discussion
Sets dst to 1 if instruction trace mode is enabled, and 0 if instruction trace mode is disabled.
insn_trace_mode_set

*Set Instruction Trace Mode*

**Syntax**

```plaintext
insn_trace_mode_set src/dst reg
```

**Discussion**

If `src/dst[0]` is 1, enables instruction trace mode. Otherwise, disables instruction trace mode. `src/dst` is set to 1 if instruction trace mode was initially enabled and 0 if it was initially disabled.

<table>
<thead>
<tr>
<th>Expansion:</th>
<th>Processor</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cx, Jx, Hx</td>
<td></td>
<td>modtc 0,0, dst</td>
</tr>
<tr>
<td></td>
<td></td>
<td>shro 1,dst,dst</td>
</tr>
<tr>
<td></td>
<td></td>
<td>and 0x1,dst,dst</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Expansion:</th>
<th>Processor</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cx, Jx, Hx</td>
<td></td>
<td>shlo 1,src/dst,src/dst</td>
</tr>
<tr>
<td></td>
<td></td>
<td>modtc 0x2,src/dst,src/dst</td>
</tr>
<tr>
<td></td>
<td></td>
<td>shro 1,src/dst,src/dst</td>
</tr>
<tr>
<td></td>
<td></td>
<td>and 0x1,src/dst,src/dst</td>
</tr>
<tr>
<td></td>
<td></td>
<td>mov g0,g0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>mov g0,g0</td>
</tr>
</tbody>
</table>
**interrupt_state**

*Read Interrupt State*

**Syntax**

```plaintext
interrupt_state  dst
                reg
```

**Discussion**

Sets `dst` to 1 if interrupts are enabled and to 0 if they are disabled.

**Expansion:**

- Processor: `Jx, Hx`
- Output: `intctl 2, dst`

---

**ip_read**

*Read Instruction Pointer*

**Syntax**

```plaintext
ip_read  dst
        reg
```

**Discussion**

Sets `dst` to the run-time address of the next instruction.

**Expansion:**

- Processor: `Cx, Jx, Hx`
- Output: `lda (ip), dst`
**ldconst**  
*Load constant*

**Syntax**

```markdown
ldconst src, dst  
lit32 reg
```

**Discussion**

Immediate values that cannot be expressed as literals must be explicitly loaded into a register before they can be used as operands for machine instructions. For integer and ordinal operands, this loading can be done with the `ldconst` directive.

The assembler selects the most efficient instruction available to place the value in the register. This instruction can be a move, add, subtract, shift, or load address, depending on the value of `src`.

<table>
<thead>
<tr>
<th>Expansion: Value of src</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1 through -31</td>
<td>subo src, 0, dst</td>
</tr>
<tr>
<td>0-31</td>
<td>mov src, dst</td>
</tr>
<tr>
<td>32-62</td>
<td>addo 31, src - 31, dst</td>
</tr>
<tr>
<td>a b†</td>
<td>shlo b, a, dst</td>
</tr>
<tr>
<td>default</td>
<td>lda src, dst</td>
</tr>
</tbody>
</table>

† 0 <= a <= 31, 0 <= b <= 31, a^b < 2^31

**NOTE.** The listing file generated by the assembler does not indicate what instruction (in the object module) substitutes for the `ldconst` directive specified in the source file. To determine what is assembled, display the instruction in the object module with the disassembler (dumper).
Example

In the following lines, you can see some of the various ways to load constants with this pseudo-instruction:

```
# ldconst and assembled instruction
ldconst 0, g5          /* mov 0,g5 */
ldconst 31, g5        /* mov 31,g5 */
ldconst 32, g5        /* addo 1,31,g5 */
addr:
    ldconst 62, g5        /* addo 31,31,g5 */
    ldconst 3<<8, g5       /* shlo 8,3,g5 */
    ldconst 0x1234, g5     /* lda 0x1234,g5 */
    ldconst -1, g5         /* subo 1,0,g5 */
    ldconst -31, g5        /* subo 31,0,g5 */
    ldconst addr, g5       /* lda addr,g5 */
```

pri_read

*Read Execution Priority*

**Syntax**

\[ \text{pri\_read} \quad \text{dst} \quad \text{reg} \]

**Discussion**

Copies the current execution priority into \(dsr[4:0]\) and zeroes into \(dsr[31:5]\).

**Expansion:**  

<table>
<thead>
<tr>
<th>Processor</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cx, Jx, Hx</td>
<td>modpc dst,0,dst</td>
</tr>
<tr>
<td></td>
<td>shro 16,dst,dst</td>
</tr>
<tr>
<td></td>
<td>and 0x1f,dst,dst</td>
</tr>
</tbody>
</table>

8-31
sw_reinit
Reinitialize Processor

Syntax
sw_reinit new_ip, new_PRCB
reg reg

Discussion
Re-initialize the processor, using new_PRCB as the new process control block. Continues execution after re-initialization beginning at the address found in new_ip.

Expansion: Processor Output

Expansion: | Processor | Output |
-----------|---------|--------|
Cx, Jx, Hx | ldconst 0x0300, SCRATCH  |
            | syscall SCRATCH, new_ip, new_PRCB |
            | # SCRATCH is any register except new_ip |
            | # or new_PRCB. |
trace_enable_set

Set Trace Enable Bit

**Syntax**

\[
\text{trace_enable_set} \quad \text{src/dst} \\
\quad \text{reg}
\]

**Discussion**

Sets trace enable bit based on value of `src/dst[0]`. Sets `src/dst` to 1 if tracing was previously enabled or 0 if it was disabled.

**Expansion:**

<table>
<thead>
<tr>
<th>Processor</th>
<th>Output</th>
</tr>
</thead>
</table>
| Cx, Jx, Hx| modpc `src/dst,0x1,src/dst`  
|           | and `src/dst,0x1,src/dst`  |
Example Programs

This chapter contains sample code, in two sections. The examples in the first section use the core instructions, and those in the second section use floating-point instructions. See the processor user’s manuals for complete lists of the instructions supported by each i960 architecture.

Note that the code shown in this chapter has not been tested on the current version of the assembler toolset. Therefore it is shown for general learning purposes only, and is not provided on the distribution media.

Examples Using the Core Instruction Set

The examples in this section use the core instructions described in Chapter 8. The example programs show:

• Code to enable interrupts to the i960 processor from an 8259A Programmable Interrupt Controller.
• Sending a breakpoint IAC message to the processor using an assembly language block in a C routine.
• Performing a bitblt code routine.
• Matrix multiplication with core instructions only.
• C-style string comparisons speed-optimized for a K-series i960 processor.
Enable and Count Interrupts From 8259A

The following source code shows how to initialize an 8259A Programmable Interrupt Controller to interrupt the i960 processor. The routine counts the number of interrupts generated.

```assembly
/* **** Enable Interrupts ****/
.globl _enable_ints
_enable_ints:
  lda cr0_address, r3          /* cntrl stat reg addr */
  ldos (r3), r4                /* cr0 is a 16 bit reg */
  lda 0xff7f, r5              /* mask for enints# bit */
  and r5, r4, r4               /* set enints# bit low */
  stos r4, (r3)
  ret

/* NOTE: the EXV complements and rotates the data bus */
/* left 3 bits. This is compensated for in 8259 read */
/* and write routines. The bits below are those that */
/* 8259 must see. */
/*----------------------------------------------------*/

/* Initialize the 8259 */
/*----------------------------------------------------*/
.globl _init_8259
_init_8259:
  /* Write ICW1: ICW4 req., 1 8259 level triggered */
  lda ICW1_ADR, g0
  lda ICW1_DATA, g1
  call _write_8259

  /* Write ICW2: Vector base of 08 */
  lda ICW2_ADR, g0
  lda ICW2_DATA, g1
  call _write_8259

  /* Write ICW4: 86/88 mode, normal EOI, non-buffered */
  /* not special fully nested */
  lda ICW4-ADR, g0
  lda ICW4-DATA, g1
  call _write_8259
```
/* Write OCW1, this is the interrupt mask register, a 0 in 
a bit in this register means that the interrupt is 
enabled. */

lda OCW1_ADR, g0
lda OCW1_DATA, g1
call _write_8259
ret

/*-----------------------------------------------------*/
/* WRITE 8259 ROUTINE */
/*-----------------------------------------------------*/
/* Write_8259 routine. Pass 8259 port address in g0 and 
the data as it should appear to the 8259 in the lower byte 
of g1. This routine will invert and rotate the data, 
write it to the 8259 and pause so that any subsequent 
accesses to the 8259 will not violate the recovery time. */

_write_8259:

lda 0x000000ff, r3     /* mask to clear bytes 1,2,3 */
and r3, g1, g1
shlo 03, g1, g1          /* shift data left 3 bits. */
lda 0x00000700, r3      /* mask all bits but 8,9,10 */
and r3, g1, r3     /* bits 8,9,10 become bits 0,1,2 */
shro 08, r3, r3    /* shift bits down to byte 0 */
or r3,g1, g1          /* combine upper 5 bits in g1 */
not g1, g1                /* invert data */
stob g1, (g0)             /* write byte to the 8259 */
bal waiting_loop       /* wait so 8259 recovery time 
guaranteed */
ret

.globl _write_count
_write_count:

lda cra_address, r3
lda 0x2a, r4
stob r4, (r3)
bal waiting_loop

lda cra_address, r3
lda 0x3a, r4
stob r4, (r3)
bal waiting_loop
lda  cra_address, r3
lda  0x1a, r4
stob  r4,  (r3)
bal  waiting_loop
lda  mra_address, r3
lda  0x02, r4
stob  r4,  (r3)
bal  waiting_loop
lda  mrb_address, r3
lda  0x07, r4
stob  r4,  (r3)
bal  waiting_loop
lda  crb_address, r3
lda  0x2a, r4
stob  r4,  (r3)
bal  waiting_loop
lda  crb_address, r3
lda  0x3a, r4
stob  r4,  (r3)
bal  waiting_loop
lda  crb_address, r3
lda  0x1a, r4
stob  r4,  (r3)
bal  waiting_loop
lda  mra_address, r3
lda  0x02, r4
stob  r4,  (r3)
bal  waiting_loop
lda  mrb_address, r3
lda  0x07, r4
stob  r4,  (r3)
bal  waiting_loop
lda  sra_address, r3
lda  0xbb, r4
stob  r4,  (r3)
bal  waiting_loop
lda srb_address, r3
lda 0xbb, r4
stob r4, (r3)
bal waiting_loop

lda input_port_address, r3
lda 0xf4, r4
stob r4, (r3)
bal waiting_loop

lda acr_address, r3
lda 0xf0, r4
stob r4, (r3)
bal waiting_loop

lda imr_address, r3
lda 0x44, r4
stob r4, (r3)
bal waiting_loop

lda ctur_address, r3
lda ctur_data, r4
stob r4, (r3)
bal waiting_loop

lda ctir_address, r3
lda ctir_data, r4
stob r4, (r3)
bal waiting_loop

lda cra_address, r3
lda 0x05, r4
stob r4, (r3)
bal waiting_loop

lda CLOCK_ADR, r3 /* zero out clock count */
lda 0, r4
st r4, (r3)
ret

/*
Wait loop required after each access to DUART registers.
*/
waiting_loop:
    lda sr0_address, r8 /* BST access;  
    DUART recovery time */
waiting_loop1:
    ldob (r8), r8  
    bx (gl4)       /* bal return */
#include "fractal.h"
#include "ints.h"
#include "mp_system.h"
.text
.globl _clock_int
_clock_int:
    mov gl4, r14  /* save bal register */
    lda cr0_address, r3
    ldos (r3), r4
    lda 0x20, r5
    or r4, r5, r4
    stos r4, (r3)
    /* update clock */
    lda CLOCK_ADR, r6
    atadd r6, 1, r7
    bal waiting_loop
    not r5, r5
    and r5, r4, r4
    stos r4, (r3)
    /*
    check clock, if time is 1 second, then signal somebody
    */
    lda SECONDS_DIVIDE, r10
    modi r10, r7, r7
    cmpibne 0, r7, cont_here
    lda 0xffffffff, r7
    lda 8(r6), r10
    lda 24(r6), r8
    stl r10, 24(r6) /* store to previous answer */
    subc r8, r10, r8
    subc r9, r11, r9
Example Programs

ldl 16(r6), r10
ldl 32(r6), r4
stl r10, 32(r6) /* store to previous answer */
subc r4, r10, r4
subc r5, r11, r5
addc r4, r8, r4
addc r5, r9, r5
/* do the fp shuffle --- */
movrl fp3, r8
cvtilr r4, fp3
movrl fp3, r4
lda 40, r11
addc r11, r6, r11
atmod r11, r7, r4 /* cumulate idle time */
movrl r8, fp3
lda 44, r11
addc r11, r6, r11
atmod r11, r7, r5 /* cumulate idle time */
lda CLOCK_PORT, r10
signal r10
/* acknowledge to 8259 that all is well */
cont_here:
  lda ADJUSTED_EOI, r4
  lda OCW2_ADR, r5
  stob r4, r5)
  mov r14, g14
  ret
waiting_loop:
  lda sr0_address, r8
waiting_loop1:
  ldob (r8), r8
  bx (g14)
.globl _no_int
_no_int:
  lda BASE_ADR, r5
  lda ADJUSTED_EOI, r4
  stob r4, (r5)
  ret
Send an IAC to the Processor

Although written in the C language, this source listing includes an ASM block that actually sends a breakpoint IAC to the processor. The code assumes that breakpoint trace mode is set in the trace controls word and that the trace enable flag of the process controls word is also set.

Figure 9-1 shows the format of the data structure used in the program.

```
/* iac structure */
struct x iac_msg {
  unsigned short  field2;
  unsigned char   field1;
  unsigned char   message_type;
  unsigned int   field3;
  unsigned int   field4;
  unsigned int   field5;
} iac_struct;

/* This routine issues an IAC message to the local processor on which the program resides. It accepts a pointer to a preformed IAC message as input, and uses the synmovq instruction to send the IAC to the processor. */

asm send_iac (struct iac_msg * base_msg)
{
  %reGlit base_msg; tmpreg myreg;
```

![Figure 9-1 IAC Message Structure](image-url)
lda 0xff000010, myreg /* load local IAC address */
synmovq myreg, base_msg
 /* issue IAC message */

%error;
}

/****************************************************/
/* Send a breakpoint IAC to the processor */
/* (don't forget to turn on breakpoints in the */
/* trace control register) */
/****************************************************/
set_breakpt(addr1, addr2)
unsigned int addr1;
unsigned int addr2;
{
  iac_struct.message_type = 0x8f;
  iac_struct.field3 = addr1;
  iac_struct.field4 = addr2;
  send_iac(&iac_struct);
}

Perform a BitBlt Operation

The following example shows a bitblt code routine. The typical size of a character stored in memory is 32 x 40 bits. Optimization techniques include:

- use of the ldconst pseudo-instruction
- use of ldq and stq to move data blocks
- register bypassing for the or instructions within the loop
- instructions are placed between compare-and-branch; the branch instruction therefore uses 0 clocks
- register loading is done before the data is actually used; other instructions are executed while waiting for the load
.text
.globl _main

_main:
  lda 0x30000, r4   /* source address in r4 */
  lda 0x40000, r5   /* destination address in r5 */
  ldconst 7, r6     /* word count in r6 */
  divi 4, r6, r7    /* quad count in r7 */
  modi 4, r6, r6    /* remainder word count in r6 */
  ldconst 4, r8     /* offset in r8 */
  ldq (r4), g0
  addi 0x10, r4, r4 /* increment source addr 4 words */
  ldconst 32, r9
  subo r8, r9, r9   /* 32 - offset */
  ldconst 0, g4     /* clear g4 for carry in */
  cmpibge 0, r7, single
      /* no quad words jump to single */

loop:
  shro r9, g4, g5   /* shift carry rt. by 32-offset */
  shlo r8, g0, g6   /* shift src1 left by offset */
  or g5, g6, g8     /* combine */
  shro r9, g0, g12  /* shift src1 right by 32-offset */
  shlo r8, g1, g13  /* shift src2 left by offset */
  or g12, g13, g9   /* combine */
  shro r9, g1, g13  /* shift src2 right by 32-offset */
  shlo r8, g2, r14  /* shift src3 left by offset */
  or g13, r14, g10  /* combine */
  shro r9, g2, g7   /* shift src3 right 32-offset */
  shlo r8, g3, g11  /* shift src4 left by offset */
  mov g3, g4        /* save src 4 for carry in */
  ldq (r4), g0      /* start next load */
  or g7, g11, g11   /* combine */
  addi 0x10, r4, r4 /* increment src addr 4 words */
  subi 1, r7, r7    /* decrement quad count */
  cmpi 0, r7        /* test if done */
  stq g8, (r5)      /* store 4 words in dest */
  addi 0x10, r5, r5 /* increment dest addr 4 words */
  bl loop           /* if not done loop back */
  cmpibge 0, r6, end /* if no remainder jump to end */

single:
  subi 0xc, r4, r4  /* get rid of extra loads */
Perform Matrix Multiplication

The following example shows an optimized version of a 1 x 3 matrix multiply, using only ordinal and integer arithmetic.

/*
   g7        input image vector pt
   g3        output sum
   r12       output line vector pt
   g0-2      a11,a12,a13      (kernel)
   g4-6      a21,a22,a23
   g8-10     a31,a32,a33
   r8-10     i1,i2,i3      (input image vector)
*/
.text
.globl _fast3x3
_fast3x3:
  mov g0, r8    /* 3x3 vector */
  mov g1, g7    /* image pointer */
  subo 1, g2, r3 /* image size */
  mov g3, r12   /* output vector point */
ldt (r8), g0  /* input 3x3 kernel */
ldt 16(r8), g4
ldt 32(r8), g8

.loop1:
  ldob (g7), r8  /* load in image and convolve */
xor g3, g3, g3
muli r8, g0, g3
ldob 1(g7), r9
muli r9, g1, r4
addi r4, g3, g3
ldob 2(g7), r10
muli r10, g2, r4
addi r4, g3, g3

ldob 640(g7), r8
muli r8, g4, r4
addi r4, g3, g3
ldob 641(g7), r9
muli r9, g5, r4
addi r4, g3, g3
ldob 642(g7), r10
muli r10, g6, r4
addi r4, g3, g3

ldob 1280(g7), r8
muli r8, g8, r4
addi r4, g3, g3
ldob 1281(g7), r9
muli r9, g9, r4
addi r4, g3, g3
ldob 1282(g7), r10
muli r10, g10, r4
addi r4, g3, g3

addo 1, g7, g7  /* increment image pointer */
addo 1, r12, r12 /* increment output line pointer */
cmpi 0, g3      /* if sum < 0, sum = 0 */
ble cont
lda 0, g3

cont:
stob g3, (r12)
cmpdeco 0, r3, r3
bl .loop1
ret
Compare Strings

The following subroutine compares two C-style null-terminated strings and returns an indication of the outcome of the comparison. The application uses the scanbyte instruction to search for the null string terminator.

```
.globl    __strcmp
.leafproc _strcmp,__strcmp
.align 2

.rett:  
    ret
__strcmp:
    lda   .rett,g14  
№ fetch first word of source_1
    mov  g14,g7       # preserve return address
    ldconst  0,g14    # conform to register conventions
    ldconst  0xff,g4  # byte extraction mask
 .wloop:   
    addo  4,g0,g0  # post-increment source_1 byte ptr
    ld    (g1), g3   # fetch word of source_2
    scanbyte 0,g5  # does word have a null byte?
    mov  g5,g2       # save a copy of the source_1 word
        .cloop     # branch if null byte encountered
    cmpo  g2,g3     # are the source words the same?
    addo  4,g1,g1  # post-increment source_2 byte ptr
    ld    (g0), g5   # fetch ahead next word of source_1
    be    .wloop     # fall thru if words are unequal
   .cloop:
    and  g4,g2,g5  # extract and compare individual bytes
    and  g4,g3,g6
    cmpbne  g5,g6,.diff # if they diff, go return 1 or -1
    cmpo  0,g6      # they are the same. Are they null?
    shlo  8,g4,g4   # position mask for next extraction
    bne   .cloop    # loop if null not encountered
```

Examples Using Floating-point Instructions

The examples in this section use the on-chip numerics instructions described in Chapter 8. The examples show:

- code optimization by reordering
- matrix multiplication with real arithmetic
- basic numerics operations using load, move, and store
- exponentiate with arbitrary exponent using rounding and scaling
- rectangular to polar conversions using trigonometric functions
- a call to the fault handler

Optimize a Numerics Application

This example shows two programs. The second, _testfast, is a speed-optimized version of the first routine, _testslow.

    .text
    .align 4
    .globl _testslow
    _testslow:
    lconst 999999, g3
    mov g0, g13    # load address pointer
    mov g1, r12    # load address pointer
    lconst 0, r3   # store loop counter
    ld1 (g13),r14
    ld1 three_point_four,r10
Example Programs

loop_begin:
    ldl (g13), r14
    mulrl r14, r10, r8
    stl r8, (r12)
    ldl 8(g13),r6
    mulrl r6, r10, r4
    stl r4, 8(r12)
    addo 1,r3,r3
    cmpi r3,g3
    ble loop_begin
    ret

.data
.align 4
three_point_four:
    # below value is 3.4 in 64 bit real format
    .word 858993459
    .word 1074475827
.text
.align 4
.globl _testfast
_testfast:
    ldconst 999999, g3
    mov g0, g13    # load address pointer
    mov g1, r14    # load address pointer
    ldconst 0, r3  # store loop counter
    ldl  (g13),r12
    ldl three_point_four,r10

loop_begin:
    ldl  8(g13), r4
    mulrl r10, r12, r8
    stl r8, (r14)
    mulrl r4, r10, r6
    stl r6, 8(r14)
    ldl  (g13), r12
    addo 1,r3,r3
    cmpi r3, g3
    ble loop_begin
    ret
Perform Matrix Multiplication

The following source code shows an optimized version of a 1 x 4 matrix multiply routine using real-valued arithmetic. The C program in the example sets up a sample matrix and uses the C version of the matrix multiply. Compare the C and assembly language versions.

Assembly Code

```assembly
/*
  r3  no. of vectors
  g7  input vector pt
  g3  output vector pt
  g0-2  a11,a12,a13,a14
  g4-6  a21,a22,a23,a24
  g8-10  a31,a32,a33,a34
  r4-7  a41,a42,a43,a44  / translation vectors /
  r8-11  i1,i2,i3,i4  /input vector/
  r12-15  o1,o2,o3,o4  /output vector/
  fast1x4 does translation and rotation of the image supplied
*/

.text
.globl  _fast1x4
_fast1x4:
  mov  g0,r8      /* 4x4 vector */
  subo  1,g2,r3   /* image size */
  movrl  g4,fp0   /* translate x */
  movr  fp0,r4
  movrl  g6,fp0   /* translate y */
  */
```

`.data
.align 4
three_point_four:
#  
# below value is 3.4 in 64 bit real format
#
.word  858993459
.word  1074475827

Example Programs

movr fp0,r5
movrl g8,fp0 /* translate z */
movr fp0,r6
mov g1,g7 /* image pointer */
ldt (r8), g0
ldt 16(r8), g4
ldt 32(r8), g8

mov r4,r4

.loop:
   ldt (g7), r8
   mulr r8, g0, fp0
   mulr r9, g4, fp1
   addr fp1, fp0, fp0
   mulr r10, g8, fp1
   addr fp1, fp0, fp0
   addr r4, fp0, r12
   mulr r8, g1, fp2
   mulr r9, g5, fp3
   addr fp3, fp2, fp2
   mulr r10, g9, fp3
   addr fp3, fp2, fp2
   addr r5, fp2, r13
   mulr r8, g2, fp0
   mulr r9, g6, fp1
   addr fp1, fp0, fp0
   mulr r10, g10, fp1
   addr fp1, fp0, fp0
   addr r6, fp0, r14
   stt r12, (g3)
   addo 12, g3, g3
   addo 12, g7, g7
   cmpdeco 0, r3, r3
   bl .loop

ret
C Code

```c
#include <stdio.h>

main ()
{
    static float a[4][4] = {
        {0.0, 0.1, 0.2, 0.3},
        {1.0, 1.1, 1.2, 1.3},
        {2.0, 2.1, 2.2, 2.3},
        {3.0, 3.1, 3.2, 3.3}};

    static float b[4] = {0.0, 0.1, 0.2, 0.3};
    float c[4];

    fast1x4(a, b, c);
}

/********************************************
/* FAST1X4                                  */
/* outer loop is the index for each column */
/* of the kernel                           */
/*                                          */
/* inner loop is the index for each row of  */
/* the kernel, and the index for the source */
/* matrix                                   */
/*                                          */
/* results are stored in a 1x4 matrix       */
/*                                          */
/* input: kernel - 4x4 matrix */
/* source - 1x4 matrix */
/* output: dest - 1x4 matrix */
/********************************************/

fast1x4 (kernel, source, dest)
float kernel [4][4];
float source[];
float dest[];
{
    int i, j;
    float temp;
```
for (i=0; i<=3; i++) {
    temp = 0.0;
    for (j=0; j<=3; j++) {
        temp += source[j] * kernel[j][i];
    }
    dest[i] = temp;
}

Perform Basic Numerics Operations

This example represents a source code fragment that does many of the basic numerics operations.

# Assume: src1 = 32-bit real value in memory
#        src2 = 96-bit extended real
#        dst uninitialized in .bss section
# (all should be appropriately aligned)
ld  src1, g0    # load 32-bit real
ldt  src2, g4   # load 96-bit extended real
movr  g0, fp0   # convert 32 to 80-bit
cpysre  fp2, g4, fp3  # copy sign
movrl  fp3, g0  # convert 80 to 64-bit real
stl  g0, dst    # store dual register long

Exponentiate With an Arbitrary Exponent

This example shows an assembly language code fragment to handle exponentiation with an arbitrary exponent.

# Assume register g0 = real exponent
roundr  g0, fp0    # fp0 = integer part
subr  fp0, g0, g0  # g0 = fractional part
expr  g0, g0       # g0 = 2^g0 - 1
addr  1.0, g0, g0  # compensate for -1
cvtri  fp0, g1 g0  # exponentiate integer
    # and scale result
Convert Between Coordinate Systems

This source code fragment converts from a rectangular to a polar coordinate system and vice-versa. These routines use several of the real arithmetic and trigonometric functions.

# Rectangular to polar conversion
# Assume x, y are 64-bit reals in memory
# r, theta are quad-aligned 96-bit locations

rect_to_polar:
  ldl  x, g0          # load x coordinate
  ldl  y, g2          # load y coordinate
  atanrl g0, g2, fp0  # fp0 = arctan y/x
  mulrl g0, g0, g0    # square x
  mulrl g2, g2, g2    # square y
  addr1 g0, g2, g4    # g4 = x^2 + y^2
  sqrtrl g4, fp1      # fp1 = sqrt g4
  movre fp0, g8       # convert theta to 96-bit
  movre fp1, g12      # convert r to 96-bit
  stt  g8, theta      # store extended angle
  stt  g12, r         # store extended radius
  ret

# Polar to rectangular conversion
# Assume:
# r, theta quad-aligned 64-bit real values
# x, y are 96-bit locations in memory

polar_to_rect:
  ldl  r, g0          # load radius
  ldl  theta, g2      # load angle
  cosrl g0, fp0       # fp0 = cos theta
  sinrl g0, fp1       # fp1 = sin theta
  mulrl fp0, g0, fp0  # fp0 = r cos theta
  mulrl fp1, g0, fp1  # fp1 = r sin theta
  movre fp0, g8       # convert x to 96-bit
  movre fp1, g12      # convert y to 96-bit
  stt  g8, x          # store extended x
  stt  g12, y         # store extended y
  ret
Retrieve Fault Record Pointer

The following routine demonstrates how to retrieve the fault record from the stack after a floating-point fault has occurred. The fault handler calls this routine immediately after the fault is signaled. The routine continues execution at the point of interruption afterwards.

The procedure `return_fault_ptr` returns the information caused by a fault to the programmer, as follows:

- The procedure returns a pointer to the fault record.
- The procedure copies all global/local registers at the time of the fault into a global structure. This structure is an array of 32 unsigned integers, which contain g0 through g15 and r0 through r15. Use a global structure to avoid passing parameters and corrupting the registers. The programmer assumes that this routine is called directly by the fault handler so it uses that knowledge to unwind the stack.
- The stack provides the linkage that you use to find the fault data, as shown in Figure 9-2.

Figure 9-2 Stack For Fault Handler

<table>
<thead>
<tr>
<th>Fault Data</th>
<th>PFP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fault Handler</td>
<td></td>
</tr>
<tr>
<td>The Procedure</td>
<td></td>
</tr>
</tbody>
</table>
.globl _return_fault_ptr
_return_fault_ptr:
    lda 0x001f0000, r8       # load pc mask
    lda 0x001f0001, r9       # load pc mask
    modpc r8, r9, r8         # set priority to MAX
                            # to avoid interrupts
    flushreg                 # make stack current
    lda  _register_set, r5
    stq  g0, (r5)            # store global registers
    stq  g4, 16(r5)
    stq  g8, 32(r5)
    stq  g12, 48(r5)
    lda  0xffffffc0, r13     # PFP mask
    ld  (pfp), r6            # chain back past previous call
    and  r6, r13, r6         # mask off return bits
    ldq  r8, 64(r5)          # load local registers
    ldq  16(r6), r8          # load local registers
    stq  r8, 80(r5)          # store local registers
    ldq  32(r6), r8          # load local registers
    stq  r8, 96(r5)          # store local registers
    ldq  48(r6), r8          # load local registers
    stq  r8, 112(r5)         # store local registers
    ldconst 48, r3           # length of fault record
    subo r3, pfp, g0         # store start of fault to g0
    ldq  32(g0), r8          # get pc, ac, ip
    stl  r8, 128(r5)         # store pc, ac
    st  r11, 136(r5)         # store ip
    ldconst 0xffffffff, r13  # load mask
    ldconst 0, r14           # turn off tracing in monitor
    modtc r13, r14, r14      # get old trace controls
    st  r14, 140(r5)         # and store to memory
    ret                      # and return it to handler

.globl _begin
.Begin:
    ldconst _register_set, r5
    ldconst 0xffffffff, r6  # load mask
    ld  140(r5), r14        # load program trace
    modtc r6, r14, r14      # set trace controls
Example Programs

Example Programs

ldconst 1, r7  # load bit
modpc r7, r7, r7  # and restore
callex (g0)  # vector off to routine
ret  # should never return,
     # but just in case
.globl _continue_execution
_continue_execution:
call restore_state
ret  # return to procedure
restore_state:
flushreg  # make stack current
     # AND.. Invalidate cache
lda _register_set, r5
ld 60(r5), r15  # get frame ptr
lda 0xffffffff, r6  # load mask
ld 132(r5), r7  # bring in stored ac
modac r6, r7, r7  # and restore
st g0, 8(r15)  # store ip in return ptr
ldq (r5), g0  # load 1st 4 globals
ldq 16(r5), g4  # load next 4 globals
ldq 32(r5), g8  # load next 4 globals
ldq 48(r5), g12  # and restore
ret
.data
.globl _register_set
_register_set:
.space 160  # reserve storage for registers
# Glossary

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>absolute expression</td>
<td>A valid assembly language symbol or expression that, when evaluated, produces a value that does not change with relocation at link time.</td>
</tr>
<tr>
<td>absolute value</td>
<td>A fixed number directly calculated by the assembler and used in the assembly. Absolute values can be used in assembly language expressions.</td>
</tr>
<tr>
<td>address space</td>
<td>The range of addresses available to a process.</td>
</tr>
<tr>
<td>addressing modes</td>
<td>Methods available for instructions to specify a memory address as an operand. The range of addressing modes for each instruction depends on the instruction type.</td>
</tr>
<tr>
<td>alignment (memory)</td>
<td>The allocation of data in memory relative to appropriate boundaries for efficient processing. For example, data words (4 bytes) must be located at memory addresses divisible by 4.</td>
</tr>
<tr>
<td>alignment (register)</td>
<td>When a single instruction accesses a dual-register group, the register specified in the instruction must be even numbered (e.g. ( g0, r2, g6 )). If an instruction accesses a triple- or quad-register group, the number of the register specified must be a multiple of four (e.g. ( g0, g4, r8 )).</td>
</tr>
<tr>
<td>ASCII-coded decimal</td>
<td>A data word containing a decimal digit (0 - 9) encoded in the four low-order bits.</td>
</tr>
<tr>
<td>assembler directive</td>
<td>A source code statement that indicates assembly information other than machine instructions to the assembler (e.g., debug information and data entries).</td>
</tr>
<tr>
<td>Term</td>
<td>Definition</td>
</tr>
<tr>
<td>----------------------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>big-endian architecture</td>
<td>The bytes follow a left-to-right order from the most significant bit to least significant bit (example: HP 9000 Series 300 workstations).</td>
</tr>
<tr>
<td>bit field</td>
<td>A contiguous series of up to 31 bits in a data word, specified by the starting bit position and field length.</td>
</tr>
<tr>
<td>burst access</td>
<td>A technique that allows the processor to execute multiple data cycles after a single address cycle.</td>
</tr>
<tr>
<td>calling convention</td>
<td>The set of instructions inserted in the object code by a language processor to handle parameter passing, stack and register use, and return values in a function call.</td>
</tr>
<tr>
<td>COFF (Common Object File Format)</td>
<td>A format for storing file and section headers, relocation information, symbol tables, and other components of an object file. When you invoke the assembler as gas960c, the assembler generates output in this format.</td>
</tr>
<tr>
<td>comparand</td>
<td>Instruction operand used in a comparison that sets the condition code.</td>
</tr>
<tr>
<td>condition code</td>
<td>Three bits that can be set by the processor as a result of comparisons and other operations. The condition code bits can be tested by running programs.</td>
</tr>
<tr>
<td>core architecture</td>
<td>A set of processor features available across all i960 processors for supporting ordinal and integer arithmetic, faults, interrupts, etc.</td>
</tr>
<tr>
<td>directive</td>
<td>See assembler directive.</td>
</tr>
<tr>
<td>double-word</td>
<td>64 bits of data. Double-word data is also called long data, and must be aligned to 8 byte boundaries for efficient use by load and store instructions.</td>
</tr>
</tbody>
</table>
ELF (Executable and Linkable Format)  The Intel 80960 ABI-compliant object module format. When invoked with the `gas960e` command, the assembler emits this format.

exception  An unusual condition that detected by the processor as the result of instruction execution. See also fault.

extended-real  IEEE standard 80-bit real number that can be processed in an 80-bit floating-point register. A 96-bit extended-real value is the same as the 80-bit extended-real value with the most-significant 16 bits ignored. A 96-bit extended-real value can be loaded into an aligned global or local triple-register group.

external reference  A symbol in an object module that refers to a location in another object module. The linker resolves external references when creating an executable module.

fatal error  An error encountered during assembly that terminates the assembly process without producing object code.

fault  An event that the processor generates to indicate that, while executing a program, a condition arose that could cause the processor to go down a wrong and possible disastrous path. One example of a fault condition is a divisor operand of zero in a divide operation; another example is an instruction with an invalid opcode.

floating-point format  IEEE standard formats for floating-point, or real, numbers. See also real number formats.

floating-point literals  The values +0.0 and +1.0.

floating-point register  80-bit registers fp0 through fp3, available on the i960 KB processor only.

global register  32-bit registers g0 through g15.
<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>half-word</td>
<td>16-bit integer or ordinal value. Half-word data is also called short data. Half-word data must be aligned on even boundaries for efficient use by the load and store instructions.</td>
</tr>
<tr>
<td>identifier</td>
<td>A symbol or name used in the source code for any purpose.</td>
</tr>
<tr>
<td>Immediate value</td>
<td>A value that is contained in the machine instruction itself (e.g., the value 10 in the instruction <code>mov 10, r5</code>) The value must be known at assembly time (i.e., cannot be unresolved).</td>
</tr>
<tr>
<td>in-circuit emulator</td>
<td>A software/hardware product used to debug embedded applications or hardware systems by emulating a particular processor.</td>
</tr>
<tr>
<td>include file</td>
<td>A source text file inserted by the assembler into the primary source text file.</td>
</tr>
<tr>
<td>instruction pointer</td>
<td>An internal processor register that contains the address of the instruction currently being executed.</td>
</tr>
<tr>
<td>instruction set</td>
<td>The set of executable instructions in a given i960 architecture.</td>
</tr>
<tr>
<td>integer</td>
<td>A positive or negative whole number or zero. The range of values that an integer can represent depends on its width (for example, short, word, or double-word).</td>
</tr>
<tr>
<td>interactive mode</td>
<td>An assembler mode of operation that allows direct input from the standard input device.</td>
</tr>
<tr>
<td>interrupt</td>
<td>A signal to the processor that an external condition requires immediate attention. An interrupt initiates a predefined handler, defined in the interrupt table, to service the condition.</td>
</tr>
<tr>
<td>J bit</td>
<td>In IEEE real number formats, a bit which is set (1) for zero and denormalized finite numbers and clear (0) otherwise. This bit can be used to detect invalid real numbers.</td>
</tr>
<tr>
<td>Term</td>
<td>Definition</td>
</tr>
<tr>
<td>----------------------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>leaf procedure</td>
<td>A local procedure that can be executed by a branch and link instruction because it doesn’t require that local registers be saved (rather than a call instruction).</td>
</tr>
<tr>
<td>linker</td>
<td>A utility used in preparing object code for execution by combining object files and resolving external references.</td>
</tr>
<tr>
<td>list file</td>
<td>A text file generated by the assembler, containing source code listing, symbol information, and other information.</td>
</tr>
<tr>
<td>literal value</td>
<td>A value in a source operand that can be used as immediate data in the instruction.</td>
</tr>
<tr>
<td>little-endian architecture</td>
<td>The bytes follow a right-to-left order from the most significant bit to least significant bit, as they do on Intel processors.</td>
</tr>
<tr>
<td>local register</td>
<td>32-bit registers r0 through r15.</td>
</tr>
<tr>
<td>location counter</td>
<td>The current address of an instruction. The location counter starts at zero and is incremented by the length of each instruction or data value in the program.</td>
</tr>
<tr>
<td>long data</td>
<td>64-bit integer or ordinal value. Long data is also called double-word data.</td>
</tr>
<tr>
<td>long-real</td>
<td>IEEE standard 64-bit floating number that can be loaded into an aligned global or local register pair.</td>
</tr>
<tr>
<td>numerics architecture</td>
<td>Processor architecture supporting hardware floating-point arithmetic and trigonometric operations available on the i960 SB/KB processors.</td>
</tr>
<tr>
<td>object code</td>
<td>Instructions and associated data for a program, in binary format. This is the output generated by the assembler and consumed by the linker.</td>
</tr>
</tbody>
</table>
object file  The file containing the object module generated by the assembler when assembly is successful. The output can be in different formats based on how you invoke the assembler (COFF for gas960c, ELF for gas960e, and b.out for gas960).

object module  The formatted object code resulting from assembly.

opcode  The portion of each machine language instruction that determines the action caused by the instruction.

operand  The argument of an assembly language directive or instruction that represents data used in the operation.

ordinal  An unsigned whole number or zero. The range of values that an ordinal can represent depends on its width (for example, short, word, or double-word).

physical address  The address of a specific hardware memory location, as sent over the bus.

pipelining  A technique that allows the processor to output the address of the next bus request during the current data cycle, maximizing bus efficiency.

position-independent code and data  The code (.text section) or data (.data or .bss section) is loaded at a run-time address that is computed as an offset from a specific location in memory.

precision  A measure of the accuracy with which a real number can be represented.

preprocessor  A program that processes an assembly language source file before the actual assembly process (for example, the macro processor mpp960).

process  An executable module that represents a complete task to the system.
<table>
<thead>
<tr>
<th><strong>program sections</strong></th>
<th>Parts of a program containing code (text section), initialized data (data section), and uninitialized data (bss section). Each section is handled separately by the linker.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>protected extension</strong></td>
<td>Filename extensions that protect the file from being overwritten by the assembler. The assembler-protected extensions are: .s, .as, and .asm.</td>
</tr>
<tr>
<td><strong>quad-word</strong></td>
<td>128 bits of data. Quad-word data must be aligned on 16-byte boundaries for efficient use by load and store instructions.</td>
</tr>
<tr>
<td><strong>real</strong></td>
<td>IEEE standard 32-bit real value that can be loaded into a single global or local register.</td>
</tr>
<tr>
<td><strong>real number formats</strong></td>
<td>IEEE standard formats for floating-point, or real, numbers: 32-bit (real), 64-bit (long-real), 80- and 96-bit (extended-real).</td>
</tr>
<tr>
<td><strong>register</strong></td>
<td>Any global register (g0 - g15), local register (r0 - r15), floating-point register (fp0 - fp3), or special function register (sf0 - sf4).</td>
</tr>
<tr>
<td><strong>register group</strong></td>
<td>A set of 2, 3, or 4 registers that participate in an instruction. See also <em>alignment (register)</em>.</td>
</tr>
<tr>
<td><strong>search path</strong></td>
<td>A list of directories used as possible pathnames to a file.</td>
</tr>
<tr>
<td><strong>short data</strong></td>
<td>16-bit integer or ordinal value. Short data is also called half-word data. Short data must be aligned on even byte boundaries for efficient use by the load and store instructions.</td>
</tr>
<tr>
<td><strong>source directory</strong></td>
<td>The directory containing your primary source file.</td>
</tr>
<tr>
<td><strong>source file</strong></td>
<td>The assembly language input to the assembler.</td>
</tr>
<tr>
<td><strong>special function register</strong></td>
<td>A 32-bit register (sf0 - sf4) used to control specific sections of the processor. These registers can be manipulated like any other register, but the contents affect the processor’s behavior directly.</td>
</tr>
<tr>
<td>Term</td>
<td>Description</td>
</tr>
<tr>
<td>------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>stack</td>
<td>A portion of memory used by the processor to store call and return information.</td>
</tr>
<tr>
<td>stack frame</td>
<td>A portion of the stack allocated by a procedure for storing temporary values until the procedure returns.</td>
</tr>
<tr>
<td>symbol table</td>
<td>A table in the object file containing information about the symbols used in a program.</td>
</tr>
<tr>
<td>system procedure</td>
<td>A procedure executed by a call system (calls) instruction. The entry point for each system procedure appears in the system procedure table.</td>
</tr>
<tr>
<td>triple-word</td>
<td>128 bits of data. Triple-word data must be aligned on 16-byte boundaries for efficient use by load and store instructions.</td>
</tr>
<tr>
<td>warning</td>
<td>An indication of an unusual condition encountered during assembly. In these situations, the assembler issues a message but continues processing the source file.</td>
</tr>
<tr>
<td>word</td>
<td>32 bits of data. Word data must be aligned on 4-byte boundaries for efficient use by the load and store instructions.</td>
</tr>
</tbody>
</table>
Index

- (hyphen), 3-1, 3-2
. (dot), location counter symbol, 5-3
/ (slash), 3-1, 3-2

A

A (Architecture) option, 4-3
.ABORT directive, 5-2, 5-10
a.out object filename, 3-4
absolute expression, defined, Glossary-1
absolute value, defined, Glossary-1
address space, defined, Glossary-1
addressing modes, defined, Glossary-1
.align directive, 5-1, 5-3, 5-11
alignment (memory), defined, Glossary-1
alignment (register), defined, Glossary-1
Allow mixed architectures (x) option, 4-21
Architecture (A) option, 4-3
architectures supported by the assembler, 1-2
arguments in assembler invocation command, 3-2
arithmetic instructions, 7-18, 7-38
ASCII-coded decimal, defined, Glossary-1
.ascii directive, 5-1, 5-6, 5-12
.asciz directive, 5-1, 5-6, 5-12
asm960 assembler invocation command, 3-1
assembler
directive, defined, Glossary-1
invocation command, 3-1
search path, default, 3-1
assembling, 3-1 thru 3-9
for the i960 Rx processor, 2-1
invoking the assembler, 3-1
specifying input files, 3-1
using assembler options, 3-1
assembly language
character set, 7-2
comments, 7-14
constants, 7-3
expressions, 7-7
identifiers, 7-3
labels, 7-6
statement format, 7-1
tokens and separators, 7-3
atomic instructions, 7-35

B

b.out object filename, 3-4
b.out OMF Support, 80960Rx, 2-7
b.out output format
and assembler invocation command, 3-1
default filename, 3-4
Big-endian (G) option, 4-7

Index-1
big-endian architecture, defined, Glossary-2
Big-Endian Support, 80960Rx, 2-7
bit and bit field instructions, 7-24
bit field, defined, Glossary-2
branch instructions, 7-27
branch pseudo-instructions, 8-2
.bss directive, 5-1, 5-4, 5-13
bswap instructions, 7-25
burst access, Glossary-2
.byte directive, 5-1, 5-6, 5-7, 5-14
byte instructions, 7-24

C
call and return instructions, 7-30
calling convention, defined, Glossary-2
 caso significance
      in assembler invocation command, 3-3
      in options, 3-1
      in UNIX and DOS, 3-2
      significance, 1-3
character constants, 7-5
COFF (Common Object File Format), defined, Glossary-2
COFF output format
      and assembler invocation command, 3-1
      default filename, 3-4
 .comm directive, 5-1, 5-7, 5-16
comparand, defined, Glossary-2
compare and branch instructions, 7-29
related option, 4-16
compare-and-jump pseudo-instructions, 8-4
comparison and classification instructions, 7-40
comparison instructions, 7-25
compatibility
      of assembler invocation syntax, 3-1
      of releases, 1-2
      with compilers, 1-2
compiler
      debugging output, 5-8
compiling
      for debugging, 5-8
condition code, defined, Glossary-2
conditional arithmetic instructions, 7-19
conditional branch instructions, 7-28
conditional faults pseudo-instructions, 8-4
core architecture, defined, Glossary-2
core instructions, summary, 7-15–7-35
Ctrl+d key combination, 3-5
customer service, 1-5

D
d (Debug symbols) option, 4-6
D (Define symbol) option, 4-4
 .data directive, 5-4, 5-17
data movement instructions, 7-15, 7-35
data type conversion instructions, 7-37
debug instructions, 7-32
Debug symbols (d) option, 4-6
debugging, directives for, 5-8
decimal constants, 7-4
decimal instructions, 7-39
 .def directive, 5-1, 5-8, 5-18
default
      assembler options, 4-1, 4-2
      instruction set, 4-3
default (continued)
output filenames, 3-4
search path, 3-1
Define symbol (D) option, 4-4
delimiters, 1-4
.desc directive, 5-1, 5-8, 5-19
dim directive, 5-8, 5-19
directives
defined, Glossary-2
for controlling the location counter, 5-3
for defining symbols, 5-7
for initializing data, 5-5
for initializing memory, 5-7
for listing control, 5-10
for optimizing, 5-9
for position independence, 5-10
for providing debugger information, 5-8
for specifying the input, 5-3
syntax, 5-2, 5-10
table of, 5-1, 5-2
documents, related, 1-3
dot (.), location counter symbol, 5-3
double directive, 5-1, 5-6, 5-20
double-word, defined, Glossary-2
.else directive, 5-1, 5-3, 5-23, 5-31
.endef directive, 5-1, 5-8, 5-18, 5-24
.endif directive, 5-1, 5-3, 5-24, 5-31
environment variables
G960ARCH, 4-3
I960ARCH, 3-7, 4-3
I960BASE, 3-8, 3-9
I960IDENT, 3-8
I960INC, 3-8
I960INC, 4-8
PATH, 3-9
using, 3-6
.equ directive, 5-1, 5-7, 5-24
tables of error messages, 4-21, 6-1
example code, 9-1–9-23
exception, defined, Glossary-3
exponential instructions, 7-42
expressions, types of, 7-10
extended arithmetic instructions, 7-19
extended directive, 5-1, 5-6, 5-25
extended-real, defined, Glossary-3
extensions
for assembly source filenames, 3-4
for file protection, 3-4
for object filenames, 3-4
external reference, defined, Glossary-3

E

e.out object filename, 3-4
.eject directive, 5-2, 5-10, 5-21
ELF output format
and assembler invocation command, 3-1
default filename, 3-4
.elf_size directive, 5-1, 5-22
.elf_type directive, 5-1, 5-23

F

fatal error, defined, Glossary-3
fault instructions, 7-31
fault, defined, Glossary-3
.file directive, 5-1, 5-26
files
  object files, 3-4
  output, specifying filename, 3-4
  source files, 3-5, 3-8
.fill directive, 5-1, 5-7, 5-27
.float directive, 5-1, 5-6, 5-28
floating-point
  constants, 7-4
  format, Glossary-3
  literals, 7-5
    defined, Glossary-3
  register, defined, Glossary-3

G
  G (Big-endian) option, 4-7
  gas960 assembler invocation command, 3-1
gas960c assembler invocation command, 3-1
gas960e assembler invocation command, 3-1
  Generate listing (L) option, 4-10
全球化 directive, 5-1, 5-7, 5-29
global register, defined, Glossary-3
global directive, 5-1, 5-7, 5-29

H
  half-word, defined, Glossary-4
  Help option (h), 4-2
  hexadecimal constants, 7-4
全球化 directive, 5-1, 5-6, 5-30, 5-47
hyphen (-), 3-1, 3-2

I
  I (Include-file search path) option, 4-8
  i (Interactive input) option, 4-9
  i960 Rx Processor, 2-1
全球化 directive, 5-2, 5-30
  identifier, defined, Glossary-4
全球化 directive, 5-1, 5-3, 5-31
全球化 directive, 5-1, 5-3, 5-31
全球化 directive, 5-1, 5-3, 5-31
全球化 directive, 5-1, 5-3, 5-31
  immediate value, Glossary-4
  in-circuit emulator, defined, Glossary-4
全球化 directive, 5-1, 5-3, 5-33
  include file, defined, Glossary-4
  Include-file search path (I) option, 4-8
input
  interactive, 3-5
  source files, 3-5
  instruction pointer, defined, Glossary-4
  instruction set, defined, Glossary-4
  instructions, core, 7-15–7-35
  instructions, numeric, 7-35–7-43
全球化 directive, 5-1, 5-6, 5-34, 5-57
integer
  constants, 7-4
    defined, Glossary-4
  interactive input, 3-6
  Interactive input (i) option, 4-9
  interactive Mode, defined, Glossary-4
  interrupt, defined, Glossary-4
Index

J-L

J bit, defined, Glossary-4
Jx Strategy, 2-1
L (Generate listing) option, 4-10
.lcomm directive, 5-1, 5-7, 5-34
.leafproc directive, 5-1, 5-9, 5-35
leaf procedure, defined, Glossary-5
.line directive, 5-1, 5-8, 5-37
.link_pix directive, 5-2, 5-10, 5-37, 5-42
linker, defined, Glossary-5
list file, defined, Glossary-5
listing control, directives for, 5-10
.list directive, 5-2, 5-10, 5-38
literal value, defined, Glossary-5
little-endian architecture, defined, Glossary-5
.ln directive, 5-1, 5-8, 5-38
load instructions, 7-16
load pseudo-instructions, 8-4
local register, Glossary-5
location counter
  defined, Glossary-5
  symbol (.), 5-3
logarithmic instructions, 7-42
logical instructions, 7-22
.lomem directive, 5-1, 5-39
long data, defined, Glossary-5
.long directive, 5-1, 5-6, 5-41, 5-57
long-real, defined, Glossary-5
.lsymb directive, 5-1, 5-7, 5-8, 5-24, 5-41

M

manuals, related, 1-3
memory address, notation, 1-5
messages, 4-21, 6-1
migration-enabling pseudo-instructions, 8-2
modulo instructions, 7-21
move instructions, 7-17

N

n (No compare-and-branch replacement)
  option, 4-16
name labels, 7-7
new features, 1-1
.nolist directive, 5-2, 5-10, 5-41
numeric labels, 7-7
numerics architecture, defined, Glossary-5
numerics instructions, summary, 7-35–7-43

O

o (Object filename) option, 4-17
object code, defined, Glossary-5
object file, defined, Glossary-6
Object filename (o) option, 4-17
object module, defined, Glossary-6
octal constants, 7-4
opcode, defined, Glossary-6
operand, defined, Glossary-6
operator precedence, 7-9, 7-10
operators, 7-8
optimizing
  directives for, 5-9
Index-6

options
  Allow mixed architectures (x), 4-21
  and arguments, 3-3
  Architecture (A), 4-3
  Big-endian (G), 4-7
  Debug symbols (d), 4-6
  Define symbol (D), 4-4
  Generate listing (L), 4-10
  Help (h), 4-2
  in assembler invocation command, 3-1
  Include-file search path (I), 4-8
  Interactive input (i), 4-9
  multiple, 3-3
  No compare-and-branch replacement (n), 4-16
  Object filename (o), 4-17
  Position independence (p), 4-18
table of, 4-1, 4-2
  Time stamp (z), 4-23
  Translate (t), 4-19
  Version (V, v960), 4-20
  Warnings (W), 4-21
  ordinal constants, 7-4
  ordinal, defined, Glossary-6
  .org directive, 5-1, 5-3, 5-41

P
  p (Position independence) option, 4-18
  physical address, defined, Glossary-6
  .pic directive, 5-2, 5-10, 5-42
  .pid directive, 5-2, 5-10, 5-42
  pipelining, defined, Glossary-6

position independence
  directives for, 5-10
  Position independence (p) option, 4-18
  position-independent code and data, defined, Glossary-6
  precision, defined, Glossary-6
  preprocessor, defined, Glossary-6
  process, defined, Glossary-6
  processor, instruction set selection, 3-7
  processor management instructions, 7-32
  program sections, defined, Glossary-7
  protected extension, defined, Glossary-7
  pseudo-instructions, 8-1 thru 8-31
  reference, 8-7 thru 8-33
  publications, related, 1-3
  punctuation, 1-4

Q-R
  quad-word, defined, Glossary-7
  real number formats, defined, Glossary-7
  real, defined, Glossary-7
  register group, defined, Glossary-7
  register, defined, Glossary-7
  registers, notation, 1-4
  remainder instructions, 7-21
  rotate instructions, 7-21
  Rx Strategy, 2-1

S
  scale instructions, 7-42
  scanbyte instruction, 7-25
  .scl directive, 5-1, 5-8, 5-43
Index

search path
  default, 3-1
  for assembler, 3-9
  include files, 3-8
search path, defined, Glossary-7
.section directive, 5-1, 5-4, 5-44
select instructions, 7-17
.set directive, 5-1, 5-7, 5-24, 5-46
shift instructions, 7-21
short data, defined, Glossary-7
.short directive, 5-1, 5-6, 5-47
sign copying instructions, 7-37
.single directive, 5-1, 5-6, 5-28, 5-48
.size directive, 5-1, 5-8, 5-49
slash (/), 3-1, 3-2
source directory, defined, Glossary-7
source file, defined, Glossary-7
source files
  description, 3-5
  interactive input, 3-5
  protection, 3-6
space between options and arguments, 3-2
.space directive, 5-1, 5-7, 5-50
special characters, 1-4
special function register, Glossary-7
.stabd directive, 5-1, 5-8, 5-51
.stabn directive, 5-1, 5-9, 5-51
.stabs directive, 5-1, 5-9, 5-51
stack frame, defined, Glossary-8
stack, defined, Glossary-8
standards, 1-2
store instructions, 7-16
string constants, 7-6
symbol table, defined, Glossary-8
synchronous instructions, 7-34
.sysproc directive, 5-1, 5-9, 5-52
system procedure, defined, Glossary-8

T
  .tag directive, 5-1, 5-8, 5-53
target expression, notation, 1-5
text directive, 5-1, 5-4, 5-54
Time stamp (z) option, 4-23
title directive, 5-2, 5-10, 5-55
Translate (t) option, 4-19
trigonometric instructions, 7-41
triple-word, defined, Glossary-8
type conversion instructions, 7-37
type directive, 5-1, 5-8, 5-55
type propagation in expressions, 7-13
typographical conventions, 1-3

U-V
  unconditional branch instructions, 7-28
V (Version) option, 4-20
v960 (Version) option, 4-20
.val directive, 5-1, 5-8, 5-56
version (V, v960) options, 4-20

W
  W (Warnings) option, 4-21
warning, defined, Glossary-8
Warnings (W) option, 4-21
word, defined, Glossary-8
.word directive, 5-1, 5-6, 5-57

**X-Z**

x (Allow mixed architectures) option, 4-21
xlate960 Assembly Language Converter, 2-8
z (Time stamp) option, 4-23