



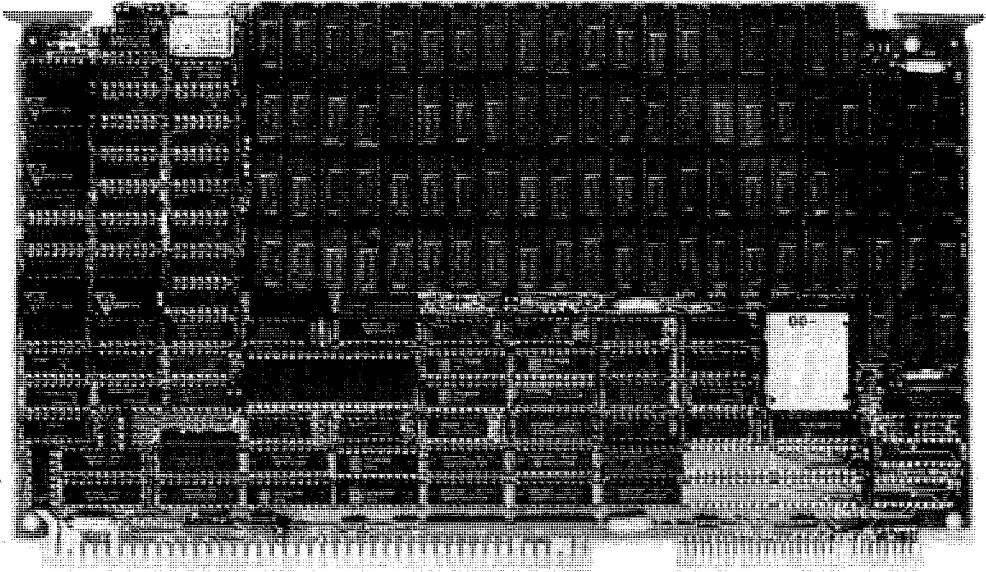
## iSBC® 012C ECC RAM BOARD

- iSBC 86, iSBC 88 RAM Expansion Through Direct, IEEE 796, MULTIBUS® Interface
- 512K Bytes of Read/Write Memory
- Single Bit Error Correction and Double Bit Error Detection Via Intel 8206 ECC Device
- Control Status Register Supports Multiple ECC Operating Modes
- Error Status Register Provides Error Logging by Host CPU Board
- Base Address Selectable on 16K Byte Boundaries
- Supports 8 or 16-Bit Transfer and 24-Bit Addressing
- Auxiliary Power Bus and Memory Protect Logic for Battery Back-Up RAM Requirements

The iSBC 012C RAM board is a member of Intel's complete line of iSBC memory and I/O Expansion boards. The board interfaces directly to any iSBC 88 or iSBC 86 Single Board Computer via the IEEE P796 MULTIBUS interface to expand system RAM capacity. The iSBC 012C board contains 512K bytes of read/write memory implemented using dynamic RAM components.

Single bit error correction and double bit error detection are provided on the iSBC 012C board via the Intel 8026 Error Checking and Correction (ECC) device. Due to the on-board ECC features of the board it is ideally suited in applications where integrity of the stored data is critical, such as financial transactions, process control and medical equipment applications.

Refresh control of the RAM array is handled on-board by the RAM Array Control Logic. Therefore, no external refresh commands are necessary.



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## FUNCTIONAL DESCRIPTION

### General

The iSBC 012C RAM board is physically and electrically compatible with the MULTIBUS interface standard, IEEE P796, as outlined in the Intel MULTIBUS specification.

### System Memory Size

Maximum system memory size with this board is 16 megabytes. On-board jumpers assign the board to one of four 4 megabyte pages. Each page is partitioned into 256 blocks of 16K bytes each. The smallest partition on the board is 16K bytes. Jumpers assign the base address (lowest 16K block) within the selected 4 megabyte page.

### Error Checking and Correcting (ECC)

Error Checking and Correction is accomplished with the Intel 8206 Error Checking and Correction device. This ECC component in conjunction with the ECC check bit RAM array provides error detection and correction of single bit errors and detection only of double bit and most multiple bit errors. The ECC circuitry can be programmed to various modes to provide full diagnostic testing of both the storage and check bit RAM arrays.

### ECC I/O Address Selection

The processor board communicates with the ECC circuitry via a single I/O port. This port is used for the Control Status Register (CSR) and the Error Status Register (ESR). The Control Status Register is programmed by the user to determine the mode of operation while the Error Status Register provides information about memory errors. The iSBC 012C RAM board is shipped with a Programmable Array Logic (PAL) device which allows selecting one of 9 possible addresses for the I/O port. The actual selection is done by jumper configuration. Additional unprogrammed locations are left in the PAL to allow application specific I/O addresses to be defined.

### Battery Back-up/Memory Protect

An auxiliary power bus is provided to allow separate power to the RAM array for systems requiring back-up of read/write memory. An active low TTL compatible memory protect signal is brought out on the auxiliary bus connector which, when asserted, disables read/write access to the RAM board. This input is provided for the protection of RAM contents during system power-down sequences.

## ERROR CHECKING AND CORRECTION

The iSBC 012C RAM board uses two special registers to pass ECC mode control and status information to and from the system master iSBC board. These registers are called the Control Status Register (CSR) and the Error Status Register (ESR).

### CONTROL STATUS REGISTER

There are six ECC modes of operation on the iSBC 012C RAM board. Each mode is obtained by software programming of the CSR from the master iSBC board. The size modes are:

- a. Interrupt on any error mode
- b. Interrupt on non-correctable error only mode
- c. Correcting mode
- d. Non-correcting mode
- e. Diagnostic mode
- f. Examine syndrome word mode

Modes (a) and (b) can be used in conjunction with (c) and (d). The six modes are described below.

**Interrupt on Any Error Mode**—In this mode the RAM board will interrupt the iSBC processor only when any error (single or multiple bit) is detected by the ECC circuitry.

**Interrupt on Non-Correctable Error Mode**—In this mode the RAM board will interrupt the iSBC processor only when a non-correctable (multiple bit) error is detected by the ECC circuitry. A multiple bit error is not correctable by the ECC circuitry.

**Correcting Mode**—In this mode the RAM board corrects any correctable error (single-bit error). Errors which are not correctable are not modified. Interrupts are generated depending on the interrupt mode selected.

**Non-Correcting Mode**—In this mode the RAM board does not correct any error. The ECC circuitry continues to check for errors, but no corrective action is taken. Interrupts continue as described previously.

**Diagnostic Mode**—This mode is used for testing the on-board ECC circuitry. In this mode the write enable strobe to the ECC RAM array is continuously disable. The diagnostic mode can be used to simulate errors and in conjunction with the "Examine Syndrome Word Mode" examine the check bits generated by the ECC circuitry.

**Examine Syndrome Word Mode**—This mode, in conjunction with the “Diagnostic Mode”, is used for testing the ECC memory. In this mode, the syndrome bits/check bits are clocked into the Error Status Register (ESR) on every memory read/write cycle, respectively. The ESR translation PROM switches to a transparent mode in the Examine Syndrome Word Mode. This allows the actual syndrome word generated by the 8206 ECC device to be examined.

**ERROR STATUS REGISTER**

This 8-bit register contains information about memory errors. The ESR reflects the latest error occurrence. Table 1 shows the status register format. Bits 5 & 6 show the failing row while bits 0 through 4 indicate which bit (of the 16-bit data word or the 6-bit ECC syndrome word) is in error. Bit 7 is always high.

Table 1

Bit		Meaning				
6	5					
0	0	Error in row	0			
0	1		1			
1	0		2			
1	1		3			
Bit						
4	3	2	1	0	Meaning	
0	0	0	0	0		
0	0	0	0	1		1
0	0	0	1	0		2
0	0	0	1	1		3
0	0	1	0	0		4
0	0	1	0	1		5
0	0	1	1	0		6
0	0	1	1	1		7
0	1	0	0	0		8
0	1	0	0	1		9
0	1	0	1	0		10
0	1	0	1	1		11
0	1	1	0	0		12
0	1	1	0	1		13
0	1	1	1	0		14
0	1	1	1	1		15
1	0	0	0	0	Error in check bit	0
1	0	0	0	0		1
1	0	0	1	0		2
1	0	0	1	1		3
1	0	1	0	0		4
0	0	1	0	1		5
1	1	1	1	0	No Error	
1	1	1	1	1	Non-correctable (multiple-bit error)	

**NOTE:**  
Bit 7 is always high

**SPECIFICATIONS**

**Word Size Supported**

8 or 16-bits

**Memory Size**

524,288 Bytes (iSBC 012C)

**Access Times (All Densities)**

Read/Full Write: 350 ns (max)

Write Byte: 530 ns (max)

**Cycle Times (All Densities)**

Read/Full Write: 460 ns (max)

Write Byte: 885 ns (max)

**NOTE:**

If an error is detected, read access time and cycle times are extended by 255 ns.

**Refresh Times**

Refresh Cycle Time: 15.6 μs

Refresh Delay Time: 760 ns

**Memory Partitioning**

Maximum System RAM size is 16M Bytes

**PAGE ADDRESS (4M BYTES)**

1 of 4 megabyte pages as follows: 0–4 megabytes; 4–8 megabytes; 8–12 megabytes; 12–16 megabytes

**BLOCK ADDRESS (16K BYTES)**

iSBC 012C RAM board—32 contiguous 16K Byte Blocks (512K Bytes)

**NOTE:**

Blocks cannot cross 4K Byte Boundary.



### BASE ADDRESS

Any 16K Byte Boundary

### Power Requirements

Voltage:  $5V_{DC} \pm 5\%$

Current: ISBC 012C 6.8A max

Standby: ISBC 012C 2.5A max

### Environmental Requirements

Operating Temperature: 0°C to 55°C

Operating Humidity: To 90% without condensation

### Physical Dimensions

Width: 12 inches (30.48 cm)

Height: 6.75 inches (17.15 cm)

Thickness: 0.50 inches (1.27 cm)

Weight: 23.5 ounces (6589 gm)

### Reference Manuals

**145183-001**—iSBC 028C/iSBC 056C/iSBC 012C Hardware Reference Manual

Manuals may be ordered from any Intel Sales Representative, Distributor Office, or from the Intel Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

### ORDERING INFORMATION

#### Part Number Description

SBC 012C 512K Byte RAM board with ECC