iSBC® 88/40A
MEASUREMENT AND CONTROL COMPUTER

- High Performance 4.8/6.67 MHz 8088 8-Bit HMOS Processor
- 12-Bit KHz Analog-to-Digital Converter with Programmable Gain Control
- 16-Bit Differential/32 Single-Ended Analog Input Channels
- Three iSBXTM MULTIMODULETM Connectors for Analog, Digital, and other I/O Expansion
- 4K Bytes Static RAM, Expandable via iSBC® 301 MULTIMODULETM RAM to 8K Bytes (1K Byte Dual-Ported)
- Four EPROM/E2PROM Sockets for up to 64K Bytes, Expandable to 128K Bytes with iSBC® 341 Expansion MULTIMODULE™
- MULTIBUS® Intelligent Slave or Multimaster

The Intel ISBC 88/40A Measurement and Control Computer is a member of Intel’s large family of Single Board Computers that takes full advantage of Intel’s VLSI technology to provide an economical self-contained computer based solution for applications in the areas of process control and data acquisition. The on-board 8088 processor with its powerful instruction set allows users of the iSBC 88/40A board to update process loops as much as 5–10 times faster than previously possible with other 8-bit microprocessors. For example, the high performance iSBC 88/40A can concurrently process and update 16 control loops in less than 200 milliseconds using a traditional PID (Proportional-Integral-Derivative) control algorithm. The iSBC 88/40A board consists of a 16 differential/32 single ended channel analog multiplexer with input protected circuits, A/D converter, programmable central processing unit, dual port and private RAM, read only memory sockets, interrupt logic, 24 channels of parallel I/O, three programmable timers and MULTIBUS control logic on a single 6.75 by 12.00-inch printed circuit card. The iSBC 88/40A board is capable of functioning by itself in a standalone system or as a multimaster or intelligent slave in a large MULTIBUS system.
FUNCTIONAL DESCRIPTION

Three Modes of Operation

The ISBC 88/40A Measurement and Control Computer (MACC) is capable of operating in one of three modes: stand-alone controller, bus multimaster or intelligent slave. A block diagram of the ISBC 88/40A Measurement and Control Computer is shown in Figure 1.

Stand-Alone Controller

The ISBC 88/40A Measurement and Control Computer may function as a stand-alone single board controller with CPU, memory and I/O elements on a single board. The on-board 4K bytes of RAM and up to 64K bytes of read only memory, as well as the analog-to-digital converter and programmable parallel I/O lines allow significant control and monitoring capabilities from a single board.

Bus Multimaster

In this mode of operation the ISBC 88/40A board may interface and control a wide variety of ISBC memory and I/O boards or even with additional ISBC 88/40 boards or other single board computer masters or intelligent slaves.

Intelligent Slave

The ISBC 88/40A board can perform as an intelligent slave to any Intel 8- or 16-bit MULTIBUS master CPU by not only offloading the master of the analog data collection, but it can also do a significant amount of pre-processing and decision-making on its own. The distribution of processing tasks to intelligent slaves frees the system master to do other system functions. The Dual port RAM with flag bytes for signaling allows the ISBC 88/40A board to process and store data without MULTIBUS memory or bus contention.

Central Processing Unit

The central processor unit for the ISBC 88/40A board is a powerful 8-bit HMOS 8088 microprocessor. By moving on-board jumpers, the user can select either a 4.8 or 6.67 MHz CPU clock rate. The ISBC 88/40A board can also run at 8 MHz by changing the CPU clock oscillator to a 24 MHz unit. For 8 MHz operation, the ISBC 88/40A board should either be the only MULTIBUS master in the system or be an intelligent slave that never directly accesses the MULTIBUS interface.
INSTRUCTION SET—The 8088 instruction repertoire includes variable length instruction format (including double operand instructions), 8-bit and 16-bit signed and unsigned arithmetic operators for binary, BCD and unpacked ASCII data, and iterative word and byte string manipulation functions. The instruction set of the 8086 is a superset of the 8080A/8085A family and with available software tools, programs written for the 8080A/8085A can be easily converted and run on the 8088 processor. Programs can also be run that are implemented on the 8088 with little or no modification.

ARCHITECTURAL FEATURES—A 4-byte instruction queue provides pre-fetching of sequential instructions and can reduce the 1.04 ms minimum instruction cycle to 417 ns (at 4.8 MHz clock rate) for queued instructions. The stack oriented architecture facilitates nested subroutines and co-routines, reentrant code and powerful interrupt handling. The memory expansion capabilities offer a 1 megabyte addressing range. The dynamic relocation scheme allows ease in segmentation of pure procedure and data for efficient memory utilization. Four segment registers (code, stack, data, extra) contain program loaded offset values which are used to map 16-bit addresses to 20-bit addresses. Each register maps 64K bytes at a time and activation of a specific register is controlled explicitly by program control and is also selected implicitly by specific functions and instructions.

Bus Structure
The iSBC 88/40A single board computer has three buses: 1) an internal bus for communicating with on-board memory, analog-to-digital converter, ISBX MULTIMODULES and I/O options; 2) the MULTIBUS system bus for referencing additional memory and I/O options, and 3) the dual-port bus which allows access to RAM from the on-board CPU and the MULTIBUS system bus. Local (on-board) accesses do not require MULTIBUS communication, making the system bus available for use by other MULTIBUS masters (i.e., DMA devices and other single board computers transferring to additional system memory). This feature allows true parallel processing in a multiprocessor environment. In addition, the MULTIBUS interface can be used for system expansion through the use of other 8- and 16-bit iSBC computers, memory and I/O expansion boards.

RAM Capabilities
DUAL-PORT RAM—The dual-port RAM of the iSBC 88/40A board consists of 1K bytes of static RAM, implemented with Intel 2114A chips. The on-board base address of this RAM is 00C00 (3K) normally; it is relocated to 01C00 (7K) when the iSBC 301 MULTIMODULE RAM is added to the protected RAM. The MULTIBUS port base address of the dual-port RAM can be jumpered to any 1K byte boundary in the 1M byte address space. The dual-port RAM can be accessed in a byte-wide fashion from the MULTIBUS system bus. When accessed from the MULTIBUS system bus, the dual-port RAM decode logic will generate INH1/ (Inhibit RAM) to allow dual-port RAM to overlay other system RAM. The dual-port control logic is designed to favor an on-board RAM access. If the dual-port is not currently performing a memory cycle for the MULTIBUS system port, only one wait state will be required. The on-board port any require more than one wait state if the dual-port RAM was busy when the on-board cycle was requested. The LOCK prefix facility of the iAPX 86/10 assembly language will disallow system bus accesses to the dual-port RAM. In addition, the on-board port to the dual-port RAM can be locked by other compatible MULTIBUS masters, which allows true symmetric semaphore operation. When the board is functioning in the master mode, the LOCK prefix will additionally disable other masters from obtaining the system bus.

PRIVATE RAM—in addition to the 1K byte dual-port RAM, there is a 3K byte section of private static RAM not accessible from the system bus. This RAM has a base address of 00000, and consists of three Intel 8186 RAM chips which are interfaced to the multiplexed address/data bus of the 8088 microprocessor. Expansion of this private RAM from 3K to 7K byte scan be accomplished by the addition of an iSBC 301 MULTIMODULE RAM (4K bytes). When the 301 is added, protected RAM extends from 0 to 7K, and the base address of the dual-port RAM is relocated from 3K (00C00) to 7K (01C00). All protected RAM accesses require one wait state. The private RAM resides on the local on-board bus, which eliminates contention problems between on-board accesses to private RAM and system bus accesses to dual-port AM. The private RAM can be battery backed (up to 16K bytes).

Additional RAM can be added by utilizing JEDEC-compatible static RAMs in the available EPROM sockets.

Parallel I/O Interface
The iSBC 88/40A single board computer contains 24 programmable parallel I/O lines implemented using the Intel 8255A Programmable Peripheral Interface. The system software is used to configure the I/O lines in any combination of unidirectional input/output and bidirectional ports indicated in Table 1. There the I/O interface may be customized to meet specific peripheral requirements. In order to take full advantage of the large number of possible I/O
configurations, sockets are provided for inter­changeable I/O line drivers and terminators. Port 2
can also accept TTL compatible peripheral drives,
such as 75461/462, 75471/472, etc. These are
open collector, high voltage drivers (up to 55 volts)
which can sink 300 mA. Hence, the flexibility of the
I/O interface is further enhanced by the capability of
selecting the appropriate combination of optional
line drivers and terminators to provide the required
sink current, polarity, and drive/termination charac­
teristics for each application. The 24 programmable
I/O lines and signal ground lines are brought out to a
50-pin edge connector that mates with flat, woven,
or round cable. This edge connector is also compati­
bile with the Intel ICSTM 920 Digital
AC Signal Conditioning/Termination Panels, for field
wiring, optical isolation and high power (up to 3 amp)
power drive.

EPROM Capabilities

Four 28-pin sockets are provided for the use of Intel
2716s, 2732s, 2764s, 27128s, future JEDEC-com­
patible 128K and 256K bit EPROMs and their respective
ROMs. When using 27128s the on-board
EPROM capacity is 64K bytes. Read only memory
expansion is available through the use of the
iSBC 341 EPROM/ROM memory expansion MULTI­
MODULE. When the iSBC 341 is used an additional
four EPROM sockets are made available, for a total
iSBC 88/40A board capacity of 128K bytes EPROM
with Intel 27128s.

E2PROM Capabilities

The four 28-pin sockets can also accommodate Intel
2817A or 2816A E2PROMs, for dynamic storage of
control loop setpoints, conversion parameters, or other
data (or programs) that change periodically but
must be kept in nonvolatile storage.

Timing Logic

The iSBC 88/40A board provides an 8254-2 Pro­
grammable Interval Timer, which contains three
independent, programmable 16-bit timers/event
counters. All three of these counters are available to
generate time intervals or event counts under soft­
ware control. The outputs of the three counters may
be independently routed to the interrupt matrix. The
inputs and outputs of timers 0 and 1 can be connect­
ed to parallel I/O lines on the J1 connector, where
they replace 8255A port C lines. The third counter is
also used for timing E2PROM write operations.

Interrupt Capability

The iSBC 88/40A board provides 9 vectored inter­
rupt levels. The highest level is NMI (Nonmaskable
Interrupt) line which is directly tied to the 8088 CPU.
This interrupt cannot be inhibited by software and is
typically used for signalling catastrophic events (i.e.,
power failure). On servicing this interrupt, program
control will be implicitly transferred through location
00008H. The Intel 8259A Programmable Interrupt
Controller (PIC) provides vectoring for the next eight
interrupt levels. As shown in Table 2, a selection of
four priority processing modes is available to the de­
signer to match system requirements. Operating
mode and priority assignments may be reconfigured
dynamically via software at any time during system
operation. The PCI accepts interrupt requests from
the programmable parallel and/or iSBX interfaces,
the programmable timers, the system bus, or directly
from peripheral equipment. The PIC then determines
which of the incoming requests is of the highest pri­
ority than the level currently being serviced, and, if
appropriate, issues an interrupt to the CPU. Any
combination of interrupt levels may be masked, via
software, by storing a single byte in the interrupt
make register of the PIC. The PIC generates a

### Table 1. Input/Output Port Modes of Operation

<table>
<thead>
<tr>
<th>Port</th>
<th>Lines (qty)</th>
<th>Mode of Operation</th>
<th>Control</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Unidirectional</td>
<td>Bidirectional</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Input</td>
<td>Output</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Latched</td>
<td>Latched &amp; Strobed</td>
</tr>
<tr>
<td>1</td>
<td>8</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>2</td>
<td>8</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>3</td>
<td>4</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

**NOTE:**
1. Part of port 3 must be used as a control port when either port 1 or port 2 are used as a latched and strobed input or a
latched and strobed output port or port 1 is used as a bidirectional port.

3-75
unique memory address for each interrupt level. These addresses are equally spaced at 4-byte intervals. This 32-byte lock may begin at any 32-byte boundary in the lowest 1K bytes of memory, and contains unique instruction pointers and code segment offset values (for expanded memory operation) for each interrupt level. After acknowledging an interrupt and obtaining advice identifier byte from the 8259A PIC, the CPU will store its status flags on the stack and execute an indirect CALL instruction through the vector location (derived from the device identifier) to the interrupt service routine.

NOTE:
The first 32 vector locations are reserved by Intel for dedicated vectors. Users who wish to maintain compatibility with present and future Intel products should not use these locations for user-defined vector addresses.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fully Nested</td>
<td>Interrupt request line priorities fixed at 0 as highest, 7 as lowest.</td>
</tr>
<tr>
<td>Auto-rotating</td>
<td>Equal priority. Each level, after receiving service, becomes the lowest priority level until next interrupt occurs.</td>
</tr>
<tr>
<td>Specific Priority</td>
<td>System software assigns lowest priority level. Priority of all other levels based in sequence numerically on this assignment.</td>
</tr>
<tr>
<td>Polled</td>
<td>System software examines priority-encoded system interrupt status via interrupt status register.</td>
</tr>
</tbody>
</table>

**INTERRUPT REQUEST GENERATION**—Interrupt requests may originate from 26 sources. Two jumper selectable interrupt requests can be automatically generated by the programmable peripheral interface when a byte of information is ready to be transferred to the CPU (i.e., input buffer is full) or a byte of information has been transferred to a peripheral device (i.e., output buffer is empty). A jumper selectable request can be generated by each of the programmable timers. An additional interrupt request line may be jumpered directly from the parallel I/O driver terminator section. Eight prioritized interrupt request lines allow the iSBC 88/40A board to recognize and service interrupts originating from peripheral boards interfaced via the MULTIBUS system bus. The fail safe timer can be selected as an interrupt source. Also, interrupts are provided from the iSBC connectors (6), end-of-conversion, PFIN and from the power line clock.

**Power-Fail Control**
Control logic is also included to accept a power-fail interrupt in conjunction with the AC-low signal from the iSBC 635, iSBC 640, and iCS 645 Power Supply or equivalent.

**iSBX™ MULTIMODULE™ Expansion Capabilities**
Three iSBX MULTIMODULE connectors are provided on the iSBC 88/40A board. Up to three single wide MULTIMODULE or one double wide and one single wide iSBX MULTIMODULE can be added to the iSBC 88/40A board. A wide variety of peripheral controllers, analog and digital expansion options are available. For more information on specific iSBX MULTIMODULES consult the Intel OEM Microcomputer System Configuration Guide.

**Processing Expansion Capabilities**
The addition of a iSBC 337 Multimodule Numeric Data Processor offers high performance integer and floating point math functions to users of the iSBC 88/40A board. The iSBC 337 incorporates the Intel 8087 and because of the MULTIMODULE implementation, it allows on-board expansion directly on the iSBC 88/40A board, eliminating the need for additional boards or floating point requirements.

**MULTIBUS® Expansion**
Memory and I/O capacity may be expanded further and additional functions added using Intel MULTIBUS compatible expansion boards. Memory may be expanded by adding user specified combination of RAM boards, EPROM boards, or memory combination boards. Input/output capacity may be increased by adding digital I/O and analog I/O MULTIBUS expansion boards. Mass storage capability may be achieved by adding single or double density diskette controllers, or hard disk controllers either through the use of expansion boards and iSBX MULTIMODULES. Modular expandable backplanes and card cages are available to support multiboard systems.

NOTE:
Certain system restrictions may be incurred by the inclusion of some of the iSBC 80 family options in an iSBC 88/40 system. Consult the Intel OEM Microcomputer System Configuration Guide for specific data.

**Analog Input Section**
The analog section of the iSBC 88/40A board receives all control signals through the local bus to
inter

iSBC® 88/40A COMPUTER

initiate channel selection, gain selection, sample and hold operation, and analog-to-digital conversion. See Figure 2.

INPUT CAPACITY—32 separate analog signals may be randomly or sequentially sampled in single-ended mode with the 32 input multiplexers and a common ground. For noisier environments, differential input mode can be configured to achieve 16 separate differential signal inputs, or 32 pseudo differential inputs.

RESOLUTION—The analog section provides 12-bit resolution with a successive approximation analog-to-digital converter. For bipolar operation (-5 to +5 or -10 to +10 volts) it provides 11 bits plus sign.

SPEED—The A-to-D converter conversion speed is 50 μs (20 kHz samples per second). Combined with the programming interface, maximum throughput via the local bus and into memory will be 55 microseconds per sample, or 18 kHz samples per second, for a single channel, a random channel, or a sequential channel scan at a gain of 1, 5 ms at a gain of 5, 250 ms at a gain of 50, and 20 ms at a gain of 250. A-to-D conversion is initiated via a programmed command from the 8088 central processor. Interrupt on end-of-conversion is a standard feature to ease programming and timing constraints.

ACCURACY—High quality components are used to achieve 12 bits resolution and accuracy of 0.035% full scale range ± 1/2 LSB at gain = 1. Offset is adjustable under program control to obtain a nominal ± 0.024% FSR ± 1/2 LSB accuracy at any fixed temperature between 0°C and 60°C (gain = 1). See specifications for other gain accuracies.

GAIN—To allow sampling of millivolt level signals such as strain gauges and thermocouples, gain is made configurable via user program commands up to 250 × (20 millivolts full scale input range). User can select gain ranges of 1 (5V), 5 (1V), 50 (100 mV), 250 (20 mV) to match his application.

OPERATIONAL DESCRIPTION—The iSBC 88/40A single board computer addresses the analog-to-digital converter by executing IN or OUT instructions to the port address. Analog-to-digital conversions can be programmed in either of two modes: 1) start conversion and poll for end-of-conversion (EOC), or 2) start conversion and wait for interrupt at end of conversion. When the conversion is complete as signaled by one of the above techniques, INput instructions read two bytes (low and high bytes) containing the 12-bit data word.

Output Command—Select input channel and start conversion.

Input Data—Read converted data (low byte) or Read converted data (high byte).

Figure 2. iSBC® 88/40 Analog Input Section

3-77
Offset Correction—At higher gains (×50, ×250) the voltage offset tempco in the A/D circuitry can sometimes cause unacceptable inaccuracies. To correct for this offset, one channel can be dedicated to be used as a reference standard. This channel can be read from the program to determine the amount of offset. The reading from this channel will then be subtracted from all other channel readings, in effect eliminating the offset tempco.

SYSTEM SOFTWARE DEVELOPMENT

The development cycle of the iSBC 88/40 board may be significantly reduced using an Intel Intellec Microcomputer Development System and Intel's FORTRAN, PASCAL, or PL/M 86/88 Software packages.

SPECIFICATIONS

Word Size
- Instruction—8, 16, or 32 bits
- Data—8 bits

Instruction Cycle Time (minimum)

<table>
<thead>
<tr>
<th>Instruction</th>
<th>8088 Clock Rate</th>
<th>Number of Clock Cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>4.8 MHz</td>
<td>6.67 MHz</td>
</tr>
<tr>
<td>In Queue</td>
<td>417 ns</td>
<td>300 ns</td>
</tr>
<tr>
<td>Not in Queue</td>
<td>1.04 ns</td>
<td>750 ns</td>
</tr>
</tbody>
</table>

MEMORY ADDRESSING

On-Board ROM/EPROM
- FE000-FFFFF (using 2716 EPROMs)
- FC000-FFFFF (using 2732 EPROMs)
- F8000-FFFFF (using 2764 EPROMs)
- F0000-FFFFF (using 27128 EPROMs)

On-Board ROM/EPROM (With iSBC 341 MULTIMODULE EPROM option installed)
- FC000-FFFFF (using 2716 EPROMs)
- F8000-FFFFF (using 2732 EPROMs)
- F0000-FFFFF (using 2764 EPROMs)
- E0000-FFFFF (using 27128 EPROMs)

On-Board RAM (CPU Access)
- 00000-00FF
- 00000-01FF (if iSBC 301 MULTIMODULE RAM option installed)

On-Board RAM

Jumpers allow 1K bytes of RAM to act as slave RAM for access by another bus master. Addressing may be set within any 1K boundary in the 1-megabyte system address space.

Slave RAM Access
- Average: 350 ns

INTERVAL TIMER

Output Frequencies

<table>
<thead>
<tr>
<th>Function</th>
<th>Single Timer</th>
<th>Dual Timers (Two Timers Cascaded)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Min</td>
<td>Max</td>
</tr>
<tr>
<td>Real-Time</td>
<td>0.977 μs</td>
<td>64 ms</td>
</tr>
<tr>
<td>Interrupt Interval</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rate</td>
<td>15.625 Hz</td>
<td>1024 KHz</td>
</tr>
<tr>
<td>Generator (Frequency)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

CPU CLOCK

- 4.8 MHz ± 0.1% or 6.67 MHz ± 0.1%. (User selectable via jumper);
- 8.0 MHz (with user installed 24 MHz oscillator)
I/O Addressing
All communications to parallel I/O ports, ISBX bus, A/D port, timers, and interrupt controller are via read and write commands from the on-board 8088 CPU.

Interface Compatibility
Parallel I/O—24 programmable lines (8 lines per port); one port includes a bidirectional bus driver. IC sockets are included for user installation of line drivers and/or I/O terminators and/or peripheral drivers as required for interface ports.

Interrupts
8088 CPU includes a non-maskable interrupt (NMI). NMI interrupt is provided for catastrophic events such as power failure. The on-board 8259A PIC provides 8-bit identifier of interrupting device to CPU. CPU multiplies identifier by four to derive vector address. Jumpers select interrupts from 26 sources without necessity of external hardware. PIC may be programmed to accommodate edge-sensitive or level-sensitive inputs.

Analog Input
16 differential (bipolar operation) or 32 single-ended (unipolar operation).

Full Scale Voltage Range—-5 to +5 volts (bipolar), 0 to +5 volts (unipolar).

NOTE:
Ranges of 0 to 10V and ±10V achievable with externally supplied ±15V power.

Gain—Program selectable for gain of 1, 5, 50, or 250.

Resolution—12 bits (11 bits plus sign for ±5, ±10 volts).

Accuracy—Including noise and dynamic errors.

Gain | 25°C |
--- | --- |
1 | ±0.035% FSR* |
5 | ±0.06% FSR* |
50 | ±0.07% FSR* |
250 | ±0.12% FSR* |

NOTE:
FSR = Full Scale Range ±1/2 LSB. Figures are in percent of full scale reading. At any fixed temperature between 0°C and 60°C, the accuracy is adjustable to ±0.05% of full scale.

Gain TC (at gain = 1)—30 PPM (typical), 56 PPM (max) per degree centigrade, 40 PPM at other gains.

Offset TC—Gain Offset TC (typical)
(in % of FSR/°C) | 1 | 0.0018% |
| 5 | 0.0036% |
| 50 | 0.024% |
| 250 | 0.12% |

Sample and Hold-Sample Time: 15 μs
Aperature-Hold Aperature Time: 120 ns
Input Overvoltage Protection: 30 volts
Input Impedance: 20 megohms (min.)
Conversion Speed: 50 μs (max.) at gain = 1
Common Mode Rejection Ratio: 60 dB (min.)

Physical Characteristics
Width: 30.48 cm (12.00 in.)
Length: 17.15 cm (6.75 in.)
Height: 1.78 cm (0.7 in.)

2.82 cm (1.13 in.) with ISBC Memory Expansion, MULTIMODULES, ISBX Numeric Data Processor or ISBX MULTIMODULES.

Electrical Requirements

Power Requirements

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Current</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Maximum</td>
</tr>
<tr>
<td>+5V</td>
<td>5.5A</td>
</tr>
<tr>
<td>+5V Aux</td>
<td>150 mA</td>
</tr>
<tr>
<td>+12V</td>
<td>120 mA</td>
</tr>
<tr>
<td>-12V</td>
<td>40 mA</td>
</tr>
</tbody>
</table>

NOTES:
1. The current requirement includes one worst case (active-standby) EPROM current.
2. If +5V Aux is supplied by the ISBC 88/40A board, the total +5V current is the sum of the +5V and the +5V Aux.

Environmental Requirements
Operating Temperature: 0° to +60°C with 6 CFM min. air flow across board
Relative Humidity: to 90% without condensation

Equipment Supplied
ISBC 88/40A Measurement and Control Computer Schematic diagram
REFERENCE MANUALS

Manuals may be ordered from an Intel sales representative, distributor office or from Intel Literature Department, 3065 Bowers Avenue, Santa Clara, California 95051.

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SBC 88/40A</td>
<td>Measurement and Control Computer</td>
</tr>
</tbody>
</table>