DRAM Controller for 40 MHz i960® CA/CF Microprocessors

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# DRAM CONTROLLER FOR 40 MHZ I960® CF MICROPROCESSORS

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1.0 INTRODUCTION

This application note describes a DRAM controller for use with the i960® CF 40 MHz microprocessor. Other application notes are available which describe DRAM controllers for the i960 Cx and Jx processors; see Section 7.0, RELATED INFORMATION for ordering information.

This DRAM controller’s design features include:

- Interleaved design
- Can use standard 70 ns DRAM SIMM
- 4-0-1-0/3-0-1-0 back-to-back/idle bus wait state burst reads up to 40 MHz
- 3-1-1-1/2-1-1-1 back-to-back/idle bus wait state burst writes up to 40 MHz
- Single clock input to state machines

This document contains some general DRAM controller theory as well as this design’s state machine definitions and timing diagrams. It also contains the PLD equations used to build and test the prototype design. All timing analysis was verified with Timing Designer*. PLD equations were generated in ABEL* as a device-independent design. Schematics were created in OrCAD*. The timing analysis, schematics and PLD files are available through Intel’s America’s Application Support BBS, at (916) 356-3600.

2.0 OVERVIEW

This section provides an overview of DRAM SIMM operation and the concept of memory interleaving. It also describes the i960 Cx microprocessor burst capabilities.

2.1 Page Mode DRAM SIMM Review

Page mode DRAM allows faster memory access by keeping the same row address while selecting random column addresses within that row. A new column address is selected by deasserting CAS while keeping RAS active and then asserting CAS with the new column address valid to the DRAM. Page mode operation works very well with burst buses in which a single address cycle can be followed by multiple data cycles.

All WE pins on each SIMM are tied to a common WE line; this line requires the use of early write cycles. In an early write cycle, write data is referenced to the falling edge of CAS, not the falling edge of WE.

Each SIMM also has four CAS lines, one for every eight (nine) bits in a 32-bit (36-bit) SIMM module. The four CAS lines control the writing to individual bytes within each SIMM.

2.2 Bank Interleaving

Interleaving significantly improves memory system performance by overlapping accesses to consecutive addresses. Two-way interleaving is accomplished by dividing the memory into two 32-bit banks (also referred to as “leaves”):

- one bank for even word addresses (A2=0)
- one bank for odd word addresses (A2=1)

The two banks are read in parallel and the data from the two banks is multiplexed onto the processor’s data bus. This overlaps the wait states of:

- the second access with the first
- the third access with the second
- the fourth access with the third

Figure 1 shows DRAM with a 2-1-1-1 quad word burst read wait state profile being interleaved to generate a 2-0-0-0 wait state system.

2.3 Burst Capabilities for 32-Bit Bus

A bus access starts by asserting ADS in the address cycle, and ends by asserting BLAST in the last data cycle. Figure 2 shows ADS and BLAST timings for a quad-word access. i960 Cx processor’s burst protocol requires:

- Quad-word and triple-word requests always start on quad word boundaries (A3 = 0, A2 = 0).
- Double-word requests always start on double word boundaries (A3 = X, A2 = 0).
• Single-word requests can start on any word boundary (A3 = X, A2 = X).
• Any request starting on an odd word boundary will never burst (A3 = X, A2 = 1).

3.0 DRAM CONTROLLER OVERVIEW

Figure 3 shows a block diagram of the DRAM Controller. The DRAM controller comprises four distinct blocks: control logic, address path, data path, and the DRAM SIMMS. This section describes each block.

3.1 Control Logic

The DRAM controller is centered around a four-bit state machine which controls DRAM bank accesses and refreshing. All timings are generated based on the four-bit state machine’s outputs. Some states are used for both read and write accesses. The state machine uses the W_RE signal from the processor to distinguish between reads and writes. This technique allows the state machine to use fewer states; therefore, fewer output bits.
3.1.1 Refresh Logic

Typically DRAMs need to be refreshed every 15.6 µs. In this design, due to power requirements needed to refresh an entire DRAM array, one bank is refreshed at a time. The DRAM controller uses an eight-bit counter to generate refresh requests. A refresh request is generated every 7.8 µs. The DRAM controller toggles between refreshing each bank every 7.8 µs which means each bank is effectively refreshed every 15.6 µs.

A refresh request has priority over a processor request. When a processor and a refresh request occur simultaneously, the DRAM controller sequences a refresh to the appropriate DRAM bank while the PENDING state machine posts the processor request. The pending request is then serviced after the refresh is completed.

An eight-bit synchronous down counter is used to generate refresh requests. The counter is clocked using the 1X_CLK clock. The REFREQ signal is asserted each time the counter reaches zero. Counting is inhibited when the counter reaches zero. The counter is reloaded with 0xff and counting resumes after the ACCESS state machine services the refresh. During reset, the counter is loaded with 0xff.

3.1.2 Clock Generation

A Motorola® MC88915 low skew CMOS PLL generates the clock signals for the DRAM controller. The MC88915 uses PCLK2 as an input, and produces four very low skew copies of PCLK2, as well as a 2x PCLK. At 40 MHz, the maximum skew between PCLK2 and any of the MC88915 outputs was calculated to be ±1 ns, while the skew between any of the individual outputs is ±750 ps under equal loading conditions. All clock lines are terminated with 22 ohm series resistors.

3.1.3 Wait State Profile

The DRAM Controller uses the processor’s READY signal to control wait states. The MCON register is initialized as follows: (NXAD = NXDA = NXDD = NXDA = 0). Table 1, Wait State Profiles, provides the wait state profiles for read and write accesses up to 40 MHz.

Back-to-back accesses require an extra wait state to meet RAS precharge time. Therefore, to meet the RAS precharge time required, the first data access for reads uses four wait state cycles as opposed to three wait state cycles for idle bus DRAM accesses. For writes, the first data access uses three wait state cycles for back-to-back accesses, as opposed to two wait state cycles for idle bus.

<table>
<thead>
<tr>
<th>Access Type</th>
<th>Wait State Profile</th>
<th>Idle Bus</th>
</tr>
</thead>
<tbody>
<tr>
<td>Quad Word Read</td>
<td>4-0-1-0</td>
<td>3-0-1-0</td>
</tr>
<tr>
<td>Triple Word Read</td>
<td>4-0-1</td>
<td>3-0-1</td>
</tr>
<tr>
<td>Double Word Read</td>
<td>4-0</td>
<td>3-0</td>
</tr>
<tr>
<td>Single Word Read</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>Quad Word Write</td>
<td>3-1-1-1</td>
<td>2-1-1-1</td>
</tr>
<tr>
<td>Triple Word Write</td>
<td>3-1-1</td>
<td>2-1-1</td>
</tr>
<tr>
<td>Double Word Write</td>
<td>3-1</td>
<td>2-1</td>
</tr>
<tr>
<td>Single Word Write</td>
<td>3</td>
<td>2</td>
</tr>
</tbody>
</table>

3.2 Address Path

Figure 4 illustrates a block diagram of the address path logic. The 2-to-1 multiplexers combine the row and column addresses into a singular row/column address that the DRAM requires. DA0E and DA0O equivalent signals are generated, one for each bank. DA0E and DA0O are generated by using A3E and A3O respectively. DA0E and DA0O are the only address bits that increment during bursts. The timing of these signals during bursts is critical for proper operation.
3.3 Data Path

As shown in Figure 5, there is one data path for reads and a separate data path for writes. The read path uses 74F257 2:1 multiplexers to prevent contention between the two DRAM banks. CAS can be active for both banks at the same time, necessitating use of the multiplexers. The multiplexer outputs are enabled only during reads by the RDEN signal. The multiplexers are switched using SELA and SELB. These signals are derived based on the states of the ACCESS state machine and address A2. The write data path consists of eight 8-bit 74F244 buffers, four for each bank. The buffer outputs are enabled by WRE and WRO.

3.4 SIMMs

The SIMM block consists of two standard 72-pin SIMM sockets, arranged as two banks: odd and even. The x36 SIMM parity bits are not used in this design. The x36 SIMMs are standard for PCs and workstations, which makes them readily available. The only penalty is more address and control line loading due to the extra DRAM devices of the x36 SIMM. All address and control lines to the SIMMs are terminated with 22 ohm resistors.

4.0 STATE MACHINES AND SIGNALS

This section describes the state machines and signals used in this design. Most of the state machines are simple and the PLD equations can be referenced in APPENDIX A. The ACCESS state machine is the most complex of all the state machines; for that reason, this application note provides more detail on the operations of this state machine. In this design, all the state machines are clocked using 1X_CLK clock (bus clock).

All PLD equations are written in ABEL. APPENDIX A, PLD EQUATIONS contains a listing of the PLD equation file. The state machine transitions described here follow the ABEL conventions for logic operators.

- ! represents NOT, bit-wise negation
- & represents AND
- # represents OR

To follow the ABEL conventions, active LOW signals (such as ADS) already have a polarity assigned. For example, in the state machines, ADS refers to the asserted state (LOW) and !ADS refers to the non-asserted state (HIGH).

4.1 ACCESS State Machine

The ACCESS state machine, the “heart” of the DRAM controller, is implemented as a four-bit state machine. See Figure 6, Basic ACCESS State Machine. It is responsible for sequencing accesses as well as refreshes to the DRAM banks.

From the IDLE state, the access state machine is sequenced based on these three events:

- Refresh requests from the counter
- DRAM requests from the processor
- PENDING state machine requests
4.2 **Pending State Machine**

The **pending** state machine is a one-bit state machine which monitors DRAM requests from the processor. This is necessary because a DRAM refresh has priority over a processor request. Therefore, this state machine is used to post the processor request. The state machine gets reset once the **access** state machine starts sequencing the pending request. The state machine generates **ACC_PEND**.

4.3 **ODDACCESS State Machine**

The **oddaccess** state machine is clocked using the 1X_CLK clock. It is a one-bit state machine which monitors the initial state of the processor’s address A2. Several state machines in this design use the output of this state machine as inputs. Address A2 from the processor indicates whether an access starts on an even or odd word boundary. The **access** state machine uses this bit extensively. It is important to latch address A2 because the processor toggles address A2 on burst accesses. This state machine generates **LA2**.

4.4 **BANKSELA State Machine**

The **banksela** state machine is a one-bit state machine which is used to control the data multiplexer, primarily to select between even or odd data during read accesses. This state machine is clocked using the 1X_CLK clock. It generates **SEL A**.

4.5 **BANKSELB State Machine**

The **bankselb** state machine is a one-bit state machine which is used to control the data multiplexer, primarily to select between even or odd data during read accesses. This state machine is clocked using the 1X_CLK clock. It generates **SEL B**.

4.6 **ADDRMUX State Machine**

The **addrmux** state machine is a one-bit state machine which is used to control the address multiplexers, primarily to select between row or column addresses. It is clocked using the 1X_CLK clock. This state machine generates **MUX**, which is a delayed version of **RAS E**. By delaying the switching of the row address by one 1X_CLK clock cycle provides ample row address hold time (t RH) required by the DRAM. The row address is selected while **MUX** is high; otherwise, the column address is selected.

4.7 **A3EVEN State Machine**

The **A3even** state machine is a one-bit state machine which is toggled on burst accesses to select the next data word (next column data). The state machine is initially loaded with the value of the processor’s address A3 and then toggled for the next data access. This state machine is clocked using 1X_CLK clock, and generates A3E. This signal is an input to the address multiplexer.

4.8 **A3ODD State Machine**

The **A3odd** state machine is a one-bit state machine and has the same functionality as the **A3even** state machine. This state machine generates **A3O**.

4.9 **RFEVENBK State Machine**

The **rfevenbk** state machine is a one-bit state machine which is used to indicate which of the two banks (even or odd) to refresh. The two banks are refreshed separately. The even bank is refreshed when the **rfevenbk** state machine is active; otherwise, the odd bank is refreshed. The output of this state machine is toggled on every refresh. This state machine generates **REFEVEN**.

4.10 **CASPIPE State Machine**

The **caspipe** state machine is a one-bit state machine which generates a pipelined CAS signal one 1X_CLK clock cycle earlier. The output of this state machine is then fed to the **CASE_B3:0** state machines where it is reconstructed to drive the CAS lines of the even bank. This state machine generates **CASE E**.

4.11 **CASPIPO State Machine**

The **caspio** state machine is a one-bit state machine which generates a pipelined CAS signal one 1X_CLK clock cycle earlier. The output of this state machine is then fed to the **CASO_B3:0** state machines where it is reconstructed to drive the CAS lines of the odd bank. This state machine generates **CASEO**.

4.12 **CASE_B3:0 State Machines**

The **case_B3:0** state machines control the CAS pins of the even bank. **CASEB0** controls the least significant byte and **CASEB3** controls the most significant byte. The **CASE B0** state machine generates **CASEB0**, and the **CASE B3** state machine generates **CASEB3**. **CASEB0** is
asserted when CASEE and the processor’s BE0 signal are asserted. CASEB3 is asserted when CASEE and the processor’s BE3 signal are asserted. CASE_B3:0 state machines are clocked using the 1X_CLK clock.

4.13 CASO_B3:0 State Machines
The CASO_B3:0 state machines control the CAS pins of the odd bank. CASO_B0 controls least significant byte and CASO_B3 controls the most significant byte. The CASO_B0 state machine generates CASOB0, and the CASO_B3 state machine generates CASOB3. CASOB0 is asserted when CASO0 and the processor’s BE0 signal are asserted. CASOB3 is asserted when CASO0 and the processor’s BE3 signal are asserted. The CASO_B3:0 state machines are clocked using the 1X_CLK clock.

4.14 REFREQ Signal
REFREQ, an active low signal, is the output of an eight-bit counter. The counter is clocked using the 1X_CLK clock. REFREQ is asserted when the counter reaches zero. The ACCESS state machine uses REFREQ to sequence refreshes.

4.15 RASEVEN State Machine
The RASEVEN state machine is a one-bit state machine which is used to generate RAS signals for the even bank. It is clocked using the 1X_CLK clock. This state machine generates RASE.

4.16 RASODD State Machine
The RASODDD state machine is a one-bit state machine which is used to generate RAS signals for the odd bank. It is clocked using the 1X_CLK clock. This state machine generates RASO.

4.17 SRASE State Machine
The SRASE state machine is a one-bit state machine which is used to monitor back-to-back DRAM accesses. It is generated by shifting RASE by one 1X_CLK clock cycle. This state machine generates SRASE. By using the state of this signal the DRAM controller can eliminate one wait state cycle for accessing the first data word. Back-to-back accesses require an extra wait state cycle to satisfy the RAS precharge time (tRP).

4.18 RDEN Signal
RDEN is asserted while a DRAM read is in progress. It controls the output enables of the data multiplexers.

4.19 WRE Signal
WRE is asserted while a DRAM write is in progress. It controls the even leaf WE lines to perform early writes. It also controls the even data path buffers output enables.

4.20 WRO Signal
WRO is asserted while a DRAM write is in progress. It controls the odd leaf WE lines to perform early writes. It also controls the odd data path buffers output enables.

5.0 DRAM CONTROLLER ACCESS FLOW
This section explains how the ACCESS state machine is sequenced while reading, writing, and refreshing DRAMs. Examples used are:
- quad-word read
- single-word read
- quad-word write
- single-word write
- refresh

The examples in this document assume back-to-back DRAM accesses or pending accesses. For example, the first data access of a DRAM request uses four wait states for reads and three wait states for writes. For idle bus accesses, the ACCESS0 state is skipped, allowing only three wait states for reads and two wait states for writes. Refer to the PLD equations in APPENDIX A. The ACCESS state machine uses SRASE to detect back-to-back accesses.

RDEN is asserted during read accesses while WRE and WRO are asserted during write accesses.

5.1 Quad-Word Read
Figure 7 shows the state diagram for a quad-word read; Figure 8 shows the timing diagram. This state diagram also shows the state machine paths for triple-, double-, and single-word reads. Single-word reads which are aligned on odd word boundaries use a different path; therefore, a separate example is used to explain that state machine path.
From the IDLE state, the machine enters the ACCESS0 state due to a processor request or a pending processor request. At the end of the IDLE state, the A3EVEN and A3ODD state machines are loaded with the processor’s address A3 and the ODDACCESS state machine is loaded with the processor’s address A2. While in the IDLE state, MUX is deasserted, which selects the row address.

At the end of the ACCESS0 state, the RASE and RASO are asserted. The machine then proceeds to the ACCESS1 state.

At the end of the ACCESS1 state, MUX is asserted. This causes the column address to be selected. CASEE is asserted, and the PENDING state machine is reset. From ACCESS1, the machine enters ACCESS2 state.

At the end of the ACCESS2 state, CASEB3:0 are asserted if CASEE and the respective Byte Enable signals from the processor are asserted. CASO is asserted if BLAST is not asserted. The machine then proceeds to the ACCESS3 state.

At the end of the ACCESS3 state, CASO3:0 are asserted if CASO and the respective Byte Enable signals from the processor are asserted, while CASEE is deasserted. The machine then proceeds to the ACCESS4 state.

The ACCESS4 state is the first or third data cycle (T4/T2) for read accesses aligned on even word boundaries. At the end of ACCESS4, CASEE is reasserted while CASEB3:0 are deasserted. CASEB3:0 are deasserted because CASEE is sampled deasserted. CASO is deasserted before leaving this state. From here, the machine can proceed to either the ACCESS5 or the IDLE state. If BLAST is asserted, the machine proceeds to the IDLE state; otherwise, to the ACCESS5 state.

The ACCESS5 state is the second or fourth data cycle (T1/T3) for read accesses. At the end of the ACCESS5 state, CASO is reasserted. CASEB3:0 are asserted if CASEE and the respective Byte Enable signals from the processor are asserted. CASO3:0 are deasserted because CASO is sampled deasserted. From here, the machine can proceed to either the ACCESS3 or the IDLE state. If BLAST is asserted, the machine proceeds to the IDLE state; otherwise, to the ACCESS3 state. The machine then proceeds to ACCESS3 state.

Figure 7. Quad-Word Read State Diagram
Figure 8. Quad-Word Read Timing Diagram
5.2 Single-Word Read

The ACCESS state machine takes a slightly different path when a read request is aligned on an odd word boundary. Figure 9 shows the state diagram for a single-word read; Figure 10 shows the timing diagram.

![Single-Word Read State Diagram](image)

A = ADS & !REFREQ & !ACC_PEND & DRAMADD & SRASE & !REFREQ & ACC_PEND
B = ADS & !REFREQ & !ACC_PEND & DRAMADD & !SRASE
C = UNCONDITIONAL
D = W_R & !LA2
E = W_R
F = W_R & !LA2
G = BLAST

At the end of ACCESS1, MUX is asserted. This causes the column address to be selected. CASOO is asserted. The PENDING state machine is reset before the machine proceeds to the ACCESS3 state.

At the end of the ACCESS3 state, CASO 3:0 are asserted if CASOO and the respective Byte Enable signals from the processor are asserted. The machine then proceeds to ACCESS4 state.

At the end of the ACCESS4 state, CASO is deasserted and the machine proceeds to the ACCESS5 state.

The ACCESS5 state is the data cycle for the read access. CASO 3:0 are deasserted. This is primarily because CASO is sampled deasserted. The machine then proceeds to the IDLE state while deasserting RASO.

![Single-Word Read Timing Diagram](image)

5.3 Quad-Word Write

Figure 11 shows the state diagram for a quad-word write. This state diagram also shows the state machine paths for triple-, double-, and single-word writes. Single-word writes which are aligned on odd word boundaries use a different path, therefore, a different example is used to explain the state machine path.

From the IDLE state, the machine enters the ACCESS0 state due to a processor request or a pending processor request. At the end of the IDLE state, the A3EVEN and A3ODD state machines are loaded with the processor’s address A3 and the ODDACCESS state machine is loaded with the processor’s address A2. MUX is deasserted in the IDLE state, which selects the row address.

At the end of the ACCESS0 state, RASO is asserted. The machine then proceeds to the ACCESS1 state.

At the end of the ACCESS1 state, MUX is asserted. This causes the column address to be selected. CASOO is asserted. The PENDING state machine is reset before the machine proceeds to the ACCESS3 state.

At the end of the ACCESS3 state, CASO 3:0 are asserted if CASOO and the respective Byte Enable signals from the processor are asserted. The machine then proceeds to ACCESS4 state.

At the end of the ACCESS4 state, CASO is deasserted and the machine proceeds to the ACCESS5 state.

The ACCESS5 state is the data cycle for the read access. CASO 3:0 are deasserted. This is primarily because CASO is sampled deasserted. The machine then proceeds to the IDLE state while deasserting RASO.
address A3, and the ODDACCESS state machine is loaded with the processor's address A2. MUX is deasserted in the IDLE state, therefore, which selects the row address.

At the end of the ACCESS0 state, RASE and RASO are asserted. The machine then proceeds to the ACCESS1 state.

At the end of the ACCESS1 state, MUX and CASEE are asserted. Asserting MUX causes the column address to be selected. From ACCESS1, the machine enters the ACCESS2 state.

At the end of the ACCESS2 state CASEE is deasserted. 

The ACCESS3 state is the first or third data cycle (T_d0 or T_d2) for write accesses which are aligned on even word boundaries (A2 = 0). At the end of the ACCESS3 state, CASEB3:0 are deasserted. This is because CASEE is sampled deasserted. CASOO is also asserted if BLAST is deasserted. From ACCESS3, the machine can proceed to either the ACCESS4 state or the IDLE state. If BLAST is asserted, the machine proceeds to the IDLE state, otherwise to the ACCESS4 state.

At the end of the ACCESS4 state, CASOO is deasserted. CASEB3:0 are asserted if CASOO and the respective Byte Enable signals from the processor are asserted. The machine then proceeds to the ACCESS5 state.

The ACCESS5 state is the second or fourth data cycle (T_d1 or T_d3) for write accesses which are aligned on even word boundaries (A2 = 0). At the end of the ACCESS5, CASEE is reasserted. CASEB3:0 are deasserted. This is because CASOO is sampled deasserted. From ACCESS5, the machine can proceed to either the ACCESS2 state or the IDLE state. If BLAST is asserted, the machine proceeds to the IDLE state, otherwise to the ACCESS2 state.

Figure 11. Quad-Word Write State Diagram
5.4 Single-Word Write

The ACCESS state machine takes a slightly different path when the write request is aligned on an odd word boundary. Figure 13 shows the state diagram for a single-word write; Figure 14 shows the timing diagram.

From the IDLE state, the machine enters the ACCESS0 state due to a processor request or a pending processor request. At the end of the IDLE state, the A3EVEN and A3ODD state machines are loaded with the processor’s address A3, and the ODDACCESS state machine is loaded with the processor’s address A2.

At the end of ACCESS0 state, RASO is asserted. The machine then proceeds to the ACCESS1 state.

At the end of ACCESS1, MUX is asserted. This causes the column address to be selected. CASO0 is also asserted. From ACCESS1, the machine enters ACCESS4 state.

At the end of the ACCESS4 state, CASO3:0 are asserted if CASO0 and the respective Byte Enable signals from the processor are asserted. CASO0 is deasserted at the end of ACCESS4. The machine then proceeds to ACCESS5 state.

The ACCESS5 state is the data cycle (T_d0) for the write access which is aligned on odd word boundary (A2 = 1). At the end of ACCESS5, CASO3:0 are deasserted. The machine then proceeds to the IDLE state.
Figure 13. Single-Word Write State Diagram
(A2 = 1)

Figure 14. Single-Word Write Timing Diagram
(A2 = 1)

5.5 Refresh Cycles

The refresh counter requests a DRAM refresh every 7.8 µs. One bank is refreshed at a time in alternation. The ACCESS state machine sequences the refresh and based on the state of the RFEVENBK state machine, either the even or the odd bank is refreshed. The following text assumes the even bank is to be refreshed, for example the RFEVENBK state machine is active. The odd bank is refreshed in a similar manner when the RFEVENBK state machine is inactive.

Figure 15 shows the refresh state diagram. From the IDLE state, the machine enters the REFRESH0 state if REFREQ is asserted. At the end of REFRESH0, CASEE is asserted. The counter is also reloaded, which deasserts REFREQ. Counting resumes on the next clock edge. The machine then proceeds to the REFRESH1 state.

At the end of the REFRESH1 state, CASEB3:0 are asserted. CASEB3:0 are asserted because CASEE is sampled asserted. The machine then proceeds to the REFRESH2 state.

At the end of the REFRESH2 state, RASE is asserted while CASEE is deasserted. The machine then proceeds to the REFRESH3 state.

At the end of the REFRESH3 state, CASEB3:0 are deasserted. This is because CASEE is sampled deasserted. The machine then proceeds to REFRESH4 and REFRESH5 state.

At the end of REFRESH5, RASE is deasserted. The machine then proceeds to the IDLE state
Figure 15. Refresh State Diagram

Figure 16. Refresh Timing Diagram
6.0 CONCLUSION

In conclusion, this application note describes a DRAM controller for use with i960® CF 40 MHz microprocessors. This DRAM Controller was built and tested for validation purposes. The PLD equations which were used to build and test the prototype design were created in ABEL. All timing analysis was verified with Timing Designer. Schematics were created with OrCAD. The timing analysis, schematics and PLD files are available through Intel’s America’s Application Support BBS, at (916) 356-3600.

7.0 RELATED INFORMATION

This application note is one of four that are related to DRAM controllers for the i960 processors. The following table shows the documents and order numbers:

<table>
<thead>
<tr>
<th>Document Name</th>
<th>App. Note #</th>
<th>Order #</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRAM Controller for the 33, 25, and 16 MHz i960® CA/CF Microprocessors</td>
<td>AP-703</td>
<td>272627</td>
</tr>
<tr>
<td>DRAM Controller for the i960® Jx Microprocessors</td>
<td>AP-712</td>
<td>272674</td>
</tr>
<tr>
<td>Simple DRAM Controller for 25/16 MHz i960® CA/CF Microprocessors</td>
<td>AP-704</td>
<td>272628</td>
</tr>
</tbody>
</table>

To receive these documents or any other available Intel literature, contact:

Intel Corporation
Literature Sales
P.O. Box 7641
Mt. Prospect IL 60056-7641
1-800-879-4683

To receive files that contain the timing analysis, schematics and PLD equations for this and the other DRAM controller application notes, contact:

Intel Corporation
America’s Application Support BBS
916-356-3600
APPENDIX A
PLD EQUATIONS

Table A-1 contains the PLD equations which were used to build and test the prototype design. Table A-2 defines signal and product term allocation. The PLD equations were created in ABEL as a device-independent design. Using the ABEL software*, a PDS file was created and subsequently imported into PLDSHELL software*. PLDSHELL was used to incorporate the design into the Altera EPX780 FLEXlogic PLD*. PLDSHELL was also used to create the JEDEC file, and to simulate the design. In addition, this appendix contains a table listing the number of product terms used by each macrocell.

This DRAM controller does not use the APK_ACTIVE signal.

Table A-1. 40MHz DRAM Controller PLD Equation (Sheet 1 of 19)

<table>
<thead>
<tr>
<th>Module</th>
<th>CX40T</th>
</tr>
</thead>
<tbody>
<tr>
<td>Title</td>
<td>'DRAM Controller for 40MHz</td>
</tr>
<tr>
<td>Source File</td>
<td>CX40T.ABL</td>
</tr>
<tr>
<td>Revision</td>
<td>Rev 0.0</td>
</tr>
<tr>
<td>Date</td>
<td>11/17/94</td>
</tr>
<tr>
<td>Designer</td>
<td>Sailesh Bissessur</td>
</tr>
<tr>
<td>Intel i960 Applications Engineering'</td>
<td></td>
</tr>
</tbody>
</table>

"2-Way Interleaved DRAM controller for the 960CF 40MHz. This design also contains logic for FLASH, HEX DISPLAY, and Software Reset
* DRAM - 0xA0000000
* FLASH - 0xFFFE0000
* HEX DISPLAY - 0xB8000000
* SW Reset - 0xB0000000

Uxx device 'iFX780_132';
inputs
CLK1 PIN; " 1x clock
CLK2 PIN;
A2 PIN; " Address A2
!EXTRST PIN; " External Reset
!CPUWAIT PIN; " Processor Wait
!ADS PIN; " Address Strobe
!BLAST PIN; " Burst Last
!W_R PIN; " Read/Write
A31 PIN; " Address A31
A30 PIN; " Address A30
A29 PIN; " Address A29
A28 PIN; " Address A28
A27 PIN; " Address A27
DCLK1 PIN; " Delayed Clock
A3 PIN; " Address A3
!BE3 PIN; " Byte Enable 3
!BE2 PIN; " Byte Enable 2
!BE1 PIN; " Byte Enable 1
!BE0 PIN; " Byte Enable 0
!APK_ACTIVE PIN; " Indicate presence of ApLink
<table>
<thead>
<tr>
<th>Pin</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>!LA2</td>
<td>reg; latched</td>
<td>A2 output</td>
</tr>
<tr>
<td>Q3</td>
<td>reg; m/c bit 3</td>
<td>Processor READY</td>
</tr>
<tr>
<td>Q2</td>
<td>reg; m/c bit 2</td>
<td></td>
</tr>
<tr>
<td>!RDEN</td>
<td>com; enables data mux</td>
<td>257 selects even odd data</td>
</tr>
<tr>
<td>!SELA</td>
<td>reg; selects even odd data</td>
<td></td>
</tr>
<tr>
<td>!SELB</td>
<td>reg; selects even odd data</td>
<td></td>
</tr>
<tr>
<td>!READY</td>
<td>reg; Processor READY</td>
<td></td>
</tr>
<tr>
<td>Q1</td>
<td>reg; m/c bit 1</td>
<td></td>
</tr>
<tr>
<td>Q0</td>
<td>reg; m/c bit 0</td>
<td></td>
</tr>
<tr>
<td>!ACC_PEND</td>
<td>reg; access pending indicator</td>
<td></td>
</tr>
<tr>
<td>!RASO</td>
<td>reg; Odd RAS</td>
<td></td>
</tr>
<tr>
<td>A3E</td>
<td>reg; Even Address Counter</td>
<td></td>
</tr>
<tr>
<td>!REFEVEN</td>
<td>reg; which bank to refresh</td>
<td></td>
</tr>
<tr>
<td>!CASEE</td>
<td>reg; Pipelined Even CAS</td>
<td></td>
</tr>
<tr>
<td>!CASOO</td>
<td>reg; Pipelined Odd CAS</td>
<td></td>
</tr>
<tr>
<td>A3O</td>
<td>reg; Odd Address Counter</td>
<td></td>
</tr>
<tr>
<td>!WAIT</td>
<td>com; wait state indicator</td>
<td></td>
</tr>
<tr>
<td>!RASE</td>
<td>reg; Even RAS</td>
<td></td>
</tr>
<tr>
<td>!MUX</td>
<td>reg; Selects Row/Column Address</td>
<td></td>
</tr>
<tr>
<td>!CASEB0</td>
<td>reg; Byte 0 Even CAS</td>
<td></td>
</tr>
<tr>
<td>!CASEB1</td>
<td>reg; Byte 1 Even CAS</td>
<td></td>
</tr>
<tr>
<td>!CASEB2</td>
<td>reg; Byte 2 Even CAS</td>
<td></td>
</tr>
<tr>
<td>!CASEB3</td>
<td>reg; Byte 3 Even CAS</td>
<td></td>
</tr>
<tr>
<td>!CASOB0</td>
<td>reg; Byte 0 Odd CAS</td>
<td></td>
</tr>
<tr>
<td>!CASOB1</td>
<td>reg; Byte 1 Odd CAS</td>
<td></td>
</tr>
<tr>
<td>!CASOB2</td>
<td>reg; Byte 2 Odd CAS</td>
<td></td>
</tr>
<tr>
<td>!CASOB3</td>
<td>reg; Byte 3 Odd CAS</td>
<td></td>
</tr>
<tr>
<td>S3</td>
<td>reg; Refresh Counter 1 bit 3</td>
<td></td>
</tr>
<tr>
<td>S2</td>
<td>reg; Refresh Counter 1 bit 2</td>
<td></td>
</tr>
<tr>
<td>S1</td>
<td>reg; Refresh Counter 1 bit 1</td>
<td></td>
</tr>
<tr>
<td>S0</td>
<td>reg; Refresh Counter 1 bit 0</td>
<td></td>
</tr>
<tr>
<td>T3</td>
<td>reg; Refresh Counter 2 bit 3</td>
<td></td>
</tr>
<tr>
<td>T2</td>
<td>reg; Refresh Counter 2 bit 2</td>
<td></td>
</tr>
<tr>
<td>T1</td>
<td>reg; Refresh Counter 2 bit 1</td>
<td></td>
</tr>
<tr>
<td>T0</td>
<td>reg; refresh Counter 2 bit 0</td>
<td></td>
</tr>
<tr>
<td>!REFREQ</td>
<td>com; Refresh Required</td>
<td></td>
</tr>
<tr>
<td>!FLASHCS</td>
<td>reg; FLASH Chip Select</td>
<td></td>
</tr>
<tr>
<td>!FLASHRD</td>
<td>reg; FLASH OE</td>
<td></td>
</tr>
<tr>
<td>!FLASHWR</td>
<td>com; FLASH WE</td>
<td></td>
</tr>
<tr>
<td>!XCROE</td>
<td>reg; XCR OE control</td>
<td></td>
</tr>
<tr>
<td>!XCRDIR</td>
<td>com; XCR DIR control</td>
<td></td>
</tr>
<tr>
<td>!SWRST</td>
<td>reg; SW Reset Indicator</td>
<td></td>
</tr>
<tr>
<td>!TRIGRST</td>
<td>reg; Triggers the 7705</td>
<td></td>
</tr>
<tr>
<td>!RESET</td>
<td>reg; System Reset</td>
<td></td>
</tr>
<tr>
<td>!WRE</td>
<td>com; Odd Bank WE</td>
<td></td>
</tr>
<tr>
<td>!WRO</td>
<td>com; Even Bank WE</td>
<td></td>
</tr>
<tr>
<td>!SRASE</td>
<td>reg; Shifted RASE</td>
<td></td>
</tr>
<tr>
<td>LED_LAT</td>
<td>reg; Hex Display Pulse</td>
<td></td>
</tr>
</tbody>
</table>

C = .C.;
X = .X.;
Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 3 of 19)

<table>
<thead>
<tr>
<th>Variable</th>
<th>Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>CYCLE</td>
<td>([Q3,Q2,Q1,Q0]);</td>
</tr>
<tr>
<td>ODDACCESS</td>
<td>([LA2]);</td>
</tr>
<tr>
<td>BANKSELA</td>
<td>([SELA]);</td>
</tr>
<tr>
<td>BANKSELB</td>
<td>([SELB]);</td>
</tr>
<tr>
<td>PENDING</td>
<td>([ACC_PEND]);</td>
</tr>
<tr>
<td>RDY</td>
<td>([READY]);</td>
</tr>
<tr>
<td>RASEVEN</td>
<td>([RASE]);</td>
</tr>
<tr>
<td>RASODD</td>
<td>([RASO]);</td>
</tr>
<tr>
<td>CAS PIPE</td>
<td>([CASEE]);</td>
</tr>
<tr>
<td>CAS PIPE O</td>
<td>([CASOO]);</td>
</tr>
<tr>
<td>ADDR MUX</td>
<td>([MUX]);</td>
</tr>
<tr>
<td>A3 EVEN</td>
<td>([A3E]);</td>
</tr>
<tr>
<td>A3 ODD</td>
<td>([A3O]);</td>
</tr>
<tr>
<td>R FEVEN BK</td>
<td>([REFEVEN]);</td>
</tr>
<tr>
<td>CASE B0</td>
<td>([CASEB0]);</td>
</tr>
<tr>
<td>CASE B1</td>
<td>([CASEB1]);</td>
</tr>
<tr>
<td>CASE B2</td>
<td>([CASEB2]);</td>
</tr>
<tr>
<td>CASE B3</td>
<td>([CASEB3]);</td>
</tr>
<tr>
<td>CASO B0</td>
<td>([CASOB0]);</td>
</tr>
<tr>
<td>CASO B1</td>
<td>([CASOB1]);</td>
</tr>
<tr>
<td>CASO B2</td>
<td>([CASOB2]);</td>
</tr>
<tr>
<td>CASO B3</td>
<td>([CASOB3]);</td>
</tr>
<tr>
<td>REF CT 2</td>
<td>([T3,T2,T1,T0]);</td>
</tr>
<tr>
<td>REF CT 1</td>
<td>([S3,S2,S1,S0]);</td>
</tr>
<tr>
<td>DRAM ADDR</td>
<td>((A31 &amp; !A30 &amp; A29 &amp; !A28 &amp; !A27);</td>
</tr>
<tr>
<td>FLASH ADDR</td>
<td>((A31 &amp; A30 &amp; A29 &amp; A28 &amp; A27);</td>
</tr>
<tr>
<td>SWRST ADDR</td>
<td>((A31 &amp; !A30 &amp; A29 &amp; A28 &amp; !A27);</td>
</tr>
<tr>
<td>LED ADDR</td>
<td>((A31 &amp; !A30 &amp; A29 &amp; A28 &amp; A27);</td>
</tr>
</tbody>
</table>

- ASSERT = \(^\text{b1}\);
- DEASSERT = \(^\text{b0}\);

<table>
<thead>
<tr>
<th>Value</th>
<th>Binary</th>
</tr>
</thead>
<tbody>
<tr>
<td>Z0</td>
<td>(^\text{b0000});</td>
</tr>
<tr>
<td>Z1</td>
<td>(^\text{b0001});</td>
</tr>
<tr>
<td>Z2</td>
<td>(^\text{b0010});</td>
</tr>
<tr>
<td>Z3</td>
<td>(^\text{b0011});</td>
</tr>
<tr>
<td>Z4</td>
<td>(^\text{b0100});</td>
</tr>
<tr>
<td>Z5</td>
<td>(^\text{b0101});</td>
</tr>
<tr>
<td>Z6</td>
<td>(^\text{b0110});</td>
</tr>
<tr>
<td>Z7</td>
<td>(^\text{b0111});</td>
</tr>
<tr>
<td>Z8</td>
<td>(^\text{b1000});</td>
</tr>
<tr>
<td>Z9</td>
<td>(^\text{b1001});</td>
</tr>
<tr>
<td>Z10</td>
<td>(^\text{b1010});</td>
</tr>
<tr>
<td>Z11</td>
<td>(^\text{b1011});</td>
</tr>
<tr>
<td>Z12</td>
<td>(^\text{b1100});</td>
</tr>
<tr>
<td>Z13</td>
<td>(^\text{b1101});</td>
</tr>
<tr>
<td>Z14</td>
<td>(^\text{b1110});</td>
</tr>
<tr>
<td>Z15</td>
<td>(^\text{b1111});</td>
</tr>
</tbody>
</table>
IDLE = ^b0000;  
ACCESS0 = ^b0001;  
ACCESS1 = ^b0010;  
ACCESS2 = ^b0011;  
ACCESS3 = ^b0100;  
ACCESS4 = ^b0101;  
ACCESS5 = ^b0110;  
ACCESS6 = ^b0111; "this state is never entered"  
ACCESS7 = ^b1000; "this state is never entered"  
REFRESH0 = ^b1001;  
REFRESH1 = ^b1010;  
REFRESH2 = ^b1011;  
REFRESH3 = ^b1100;  
REFRESH4 = ^b1101;  
REFRESH5 = ^b1110;  
REFRESH6 = ^b1111; "this state is never entered"  

*Holds state of A2 of the processor  
state_diagram ODDACCESS  
state ASSERT:  
  if((CYCLE == IDLE) & A2) then DEASSERT  
else  
  ASSERT;  
state DEASSERT:  
  if((CYCLE == IDLE) & !A2) then ASSERT  
else  
  DEASSERT;  

*Even byte 0 CAS  
state_diagram CASE_B0  
state ASSERT:  
  if(!Q3 & !CASEE) then DEASSERT  
else  
  if(Q3 & !CASEE) then DEASSERT  
else  
  ASSERT;  
state DEASSERT:  
  if(!(Q3 & !CASEE & WAIT & CASEE & !BE0)) then ASSERT  
else  
  if(!Q3 & W_R & !WAIT & CASEE & BE0 & !BLAST) then ASSERT  
else  
  if(!(Q3 & W_R & CASEE & BE0)) then ASSERT  
else  
  if(Q3 & CASEE) then ASSERT  
else  
  DEASSERT;
<table>
<thead>
<tr>
<th>State Diagram</th>
<th>Case (1)</th>
<th>Case (2)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Assert</strong></td>
<td>if(!Q3 &amp; !CASEE) then DEASSERT</td>
<td>if(!Q3 &amp; !CASEE) then DEASSERT</td>
</tr>
<tr>
<td></td>
<td>else if(Q3 &amp; !CASEE) then DEASSERT</td>
<td>else if(Q3 &amp; !CASEE) then DEASSERT</td>
</tr>
<tr>
<td></td>
<td>else ASSERT;</td>
<td>else ASSERT;</td>
</tr>
<tr>
<td><strong>Deassert</strong></td>
<td>if(!Q3 &amp; W_R &amp; WAIT &amp; CASEE &amp; BE1) then ASSERT</td>
<td>if(!Q3 &amp; W_R &amp; WAIT &amp; CASEE &amp; BE2) then ASSERT</td>
</tr>
<tr>
<td></td>
<td>else if(!Q3 &amp; W_R &amp; !WAIT &amp; CASEE &amp; BE1 &amp; !BLAST) then ASSERT</td>
<td>else if(!Q3 &amp; W_R &amp; !WAIT &amp; CASEE &amp; BE2 &amp; !BLAST) then ASSERT</td>
</tr>
<tr>
<td></td>
<td>else if(!Q3 &amp; W_R &amp; CASEE &amp; BE1) then ASSERT</td>
<td>else if(!Q3 &amp; W_R &amp; CASEE &amp; BE2) then ASSERT</td>
</tr>
<tr>
<td></td>
<td>else if(Q3 &amp; CASEE) then ASSERT</td>
<td>else if(Q3 &amp; CASEE) then ASSERT</td>
</tr>
<tr>
<td></td>
<td>else DEASSERT;</td>
<td>else DEASSERT;</td>
</tr>
</tbody>
</table>
Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 6 of 19)

**Even byte 3 CAS**

```
state_diagram CASE_B3
  state ASSERT:
   if(!Q3 & !CASEE) then DEASSERT
   else if(Q3 & !CASEE) then DEASSERT
   else ASSERT;
  state DEASSERT:
   if(!Q3 & W_R & WAIT & CASEE & BE3) then ASSERT
   else if(!Q3 & W_R & !WAIT & CASEE & BE3 & !BLAST) then ASSERT
   else if(!Q3 & !W_R & CASEE & BE3) then ASSERT
   else if(Q3 & CASEE) then ASSERT
   else DEASSERT;
```

**Odd byte 0 CAS**

```
state_diagram CASO_B0
  state ASSERT:
   if(!Q3 & !CASOO) then DEASSERT
   else if(Q3 & !CASOO) then DEASSERT
   else ASSERT;
  state DEASSERT:
   if(!Q3 & W_R & WAIT & CASOO & BE0 & BLAST & !LA2) then ASSERT
   else if(!Q3 & W_R & WAIT & CASOO & BE0 & !BLAST & LA2) then ASSERT
   else if(!Q3 & !W_R & CASOO & BE0) then ASSERT
   else if(Q3 & CASOO) then ASSERT
   else DEASSERT;
```
Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 7 of 19)

<table>
<thead>
<tr>
<th>State Diagram</th>
<th>State</th>
<th>Condition</th>
<th>Action</th>
</tr>
</thead>
<tbody>
<tr>
<td>CASO_B1</td>
<td>ASSERT</td>
<td>!Q3 &amp; CAS0</td>
<td>DEASSERT</td>
</tr>
<tr>
<td></td>
<td>ASSERT</td>
<td>Q3 &amp; CAS0</td>
<td>DEASSERT</td>
</tr>
<tr>
<td></td>
<td>DEASSERT</td>
<td>!Q3 &amp; W_R &amp; WAIT &amp; CAS0 &amp; BE1 &amp; BLAST &amp; !LA2</td>
<td>ASSERT</td>
</tr>
<tr>
<td></td>
<td>DEASSERT</td>
<td>!Q3 &amp; W_R &amp; WAIT &amp; CAS0 &amp; BE1 &amp; !BLAST &amp; LA2</td>
<td>ASSERT</td>
</tr>
<tr>
<td></td>
<td>DEASSERT</td>
<td>!Q3 &amp; W_R &amp; CAS0 &amp; BE1</td>
<td>DEASSERT</td>
</tr>
<tr>
<td></td>
<td>DEASSERT</td>
<td>Q3 &amp; CAS0</td>
<td>ASSERT</td>
</tr>
<tr>
<td>CASO_B2</td>
<td>ASSERT</td>
<td>!Q3 &amp; CAS0</td>
<td>DEASSERT</td>
</tr>
<tr>
<td></td>
<td>ASSERT</td>
<td>Q3 &amp; CAS0</td>
<td>DEASSERT</td>
</tr>
<tr>
<td></td>
<td>DEASSERT</td>
<td>!Q3 &amp; W_R &amp; WAIT &amp; CAS0 &amp; BE2 &amp; BLAST &amp; !LA2</td>
<td>ASSERT</td>
</tr>
<tr>
<td></td>
<td>DEASSERT</td>
<td>!Q3 &amp; W_R &amp; WAIT &amp; CAS0 &amp; BE2 &amp; !BLAST &amp; LA2</td>
<td>ASSERT</td>
</tr>
<tr>
<td></td>
<td>DEASSERT</td>
<td>!Q3 &amp; W_R &amp; CAS0 &amp; BE2</td>
<td>DEASSERT</td>
</tr>
<tr>
<td></td>
<td>DEASSERT</td>
<td>Q3 &amp; CAS0</td>
<td>ASSERT</td>
</tr>
<tr>
<td>State Diagram: CASO_B3</td>
<td>State Diagram: PENDING</td>
<td>State Diagram: RFEVENBK</td>
<td></td>
</tr>
<tr>
<td>------------------------</td>
<td>------------------------</td>
<td>------------------------</td>
<td></td>
</tr>
<tr>
<td><strong>State Diagram CASO_B3</strong></td>
<td><strong>State Diagram PENDING</strong></td>
<td><strong>State Diagram RFEVENBK</strong></td>
<td></td>
</tr>
<tr>
<td><strong>State ASSERT:</strong></td>
<td><strong>State ASSERT:</strong></td>
<td><strong>State ASSERT:</strong></td>
<td></td>
</tr>
<tr>
<td>if(!Q3 &amp; !CASOO) then DEASSERT</td>
<td>if(CYCLE == ACCESS1) then DEASSERT</td>
<td>if((CYCLE == REFRESH2)) then DEASSERT</td>
<td></td>
</tr>
<tr>
<td>else</td>
<td>else</td>
<td>else</td>
<td></td>
</tr>
<tr>
<td>if(Q3 &amp; !CASOO) then DEASSERT</td>
<td>assert</td>
<td>if((CYCLE == REFRESH2)) then DEASSERT</td>
<td></td>
</tr>
<tr>
<td>else</td>
<td>assert</td>
<td>else</td>
<td></td>
</tr>
<tr>
<td>DEASSERT;</td>
<td>DEASSERT;</td>
<td>DEASSERT;</td>
<td></td>
</tr>
</tbody>
</table>

*Odd byte 3 CAS

*Keeps track of any pending accesses

*Indicates which Bank is to be refreshed next when !REFREQ becomes active

---

Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 8 of 19)
Table A-1. 40 MHz DRAM Controller PLD Equation

---

*Selects even or odd data

**state_diagram BANKSEL A**

```
state ASSERT:
  if(CYCLE == ACCESS4) then DEASSERT
else
  if((CYCLE == IDLE) & W_R & A2) then DEASSERT
else
  ASSERT;

state DEASSERT:
  if((CYCLE == ACCESS3) & W_R) then ASSERT
else
  if((CYCLE == IDLE) & W_R & !A2) then ASSERT
else
  DEASSERT;
```

*Selects even or odd data

**state_diagram BANKSEL B**

```
state ASSERT:
  if(CYCLE == ACCESS4) then DEASSERT
else
  if((CYCLE == IDLE) & W_R & A2) then DEASSERT
else
  ASSERT;

state DEASSERT:
  if((CYCLE == ACCESS3) & W_R) then ASSERT
else
  if((CYCLE == IDLE) & W_R & !A2) then ASSERT
else
  DEASSERT;
```

*Generates READY to the processor

**state_diagram RDY**

```
state ASSERT:
  if((CYCLE == ACCESS4) & W_R & BLAST) then DEASSERT
else
  if((CYCLE == ACCESS5)) then DEASSERT
else
  if((CYCLE == ACCESS3)) then DEASSERT
else
  ASSERT;

state DEASSERT:
  if((CYCLE == ACCESS2) & !W_R) then ASSERT
else
  if((CYCLE == ACCESS3) & W_R & LA2) then ASSERT
else
  if((CYCLE == ACCESS4) & W_R & !LA2) then ASSERT
else
  if((CYCLE == ACCESS4) & !W_R) then ASSERT
else
  DEASSERT;
```
### Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 10 of 19)

- **Even RAS**

  ```
  state_diagram RASEVEN
  state ASSERT:
    if((CYCLE == ACCESS3) & !W_R & BLAST) then DEASSERT
    else
      if((CYCLE == ACCESS4) & W_R & BLAST & LA2) then DEASSERT
      else
        if((CYCLE == ACCESS5) & BLAST) then DEASSERT
        else
          if((CYCLE == REFRESH5)) then DEASSERT
          else
            ASSERT;
  state DEASSERT:
    if((CYCLE == IDLE) & ADS & !REFREQ & !ACC_PEND & DRAMADDR & !SRASE) then ASSERT
    else
      if((CYCLE == ACCESS0)) then ASSERT
      else
        if((CYCLE == REFRESH2) & !REFEVEN) then ASSERT
        else
          DEASSERT;
  ```

- **Odd RAS**

  ```
  state_diagram RASODD
  state ASSERT:
    if((CYCLE == ACCESS3) & !W_R & BLAST) then DEASSERT
    else
      if((CYCLE == ACCESS4) & W_R & BLAST & LA2) then DEASSERT
      else
        if((CYCLE == ACCESS5) & BLAST) then DEASSERT
        else
          if((CYCLE == REFRESH5)) then DEASSERT
          else
            ASSERT;
  state DEASSERT:
    if((CYCLE == IDLE) & ADS & !REFREQ & !ACC_PEND & DRAMADDR & !SRASE) then ASSERT
    else
      if((CYCLE == ACCESS0)) then ASSERT
      else
        if((CYCLE == REFRESH2) & !REFEVEN) then ASSERT
        else
          DEASSERT;
  ```
### Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 11 of 19)

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<tr>
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<th>Even CAS PIPE</th>
<th>Asserting Events</th>
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<td>CASPIPE</td>
<td></td>
</tr>
<tr>
<td>State</td>
<td>ASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>if ((CYCLE == ACCESS2) &amp; !W.R) then DEASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>else</td>
<td></td>
</tr>
<tr>
<td></td>
<td>if ((CYCLE == ACCESS3) &amp; W.R) then DEASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>else</td>
<td></td>
</tr>
<tr>
<td></td>
<td>if ((CYCLE == ACCESS5) &amp; BLAST &amp; W.R) then DEASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>else</td>
<td></td>
</tr>
<tr>
<td></td>
<td>if ((CYCLE == REFRESH2)) then DEASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>else</td>
<td></td>
</tr>
<tr>
<td>State</td>
<td>DEASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>if ((CYCLE == ACCESS1) &amp; LA2) then ASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>else</td>
<td></td>
</tr>
<tr>
<td></td>
<td>if ((CYCLE == ACCESS4) &amp; W.R &amp; LA2 &amp; !BLAST) then ASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>else</td>
<td></td>
</tr>
<tr>
<td></td>
<td>if ((CYCLE == ACCESS5) &amp; !W.R &amp; !BLAST) then ASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>else</td>
<td></td>
</tr>
<tr>
<td></td>
<td>if ((CYCLE == REFRESH0) &amp; REFEVEN) then ASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>else</td>
<td></td>
</tr>
<tr>
<td>State Diagram</td>
<td>CASPIPO</td>
<td></td>
</tr>
<tr>
<td>State</td>
<td>ASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>if ((CYCLE == ACCESS4)) then DEASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>else</td>
<td></td>
</tr>
<tr>
<td></td>
<td>if ((CYCLE == REFRESH2)) then DEASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>else</td>
<td></td>
</tr>
<tr>
<td>State</td>
<td>DEASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>if ((CYCLE == ACCESS2) &amp; W.R &amp; LA2 &amp; !BLAST) then ASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>else</td>
<td></td>
</tr>
<tr>
<td></td>
<td>if ((CYCLE == ACCESS3) &amp; !W.R &amp; !BLAST) then ASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>else</td>
<td></td>
</tr>
<tr>
<td></td>
<td>if ((CYCLE == ACCESS1) &amp; !LA2) then ASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>else</td>
<td></td>
</tr>
<tr>
<td></td>
<td>if ((CYCLE == ACCESS5) &amp; !BLAST &amp; W.R) then ASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>else</td>
<td></td>
</tr>
<tr>
<td></td>
<td>if ((CYCLE == REFRESH0) &amp; !REFEVEN) then ASSERT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>else</td>
<td></td>
</tr>
</tbody>
</table>

*Pipelined Even CAS*

*Pipelined Odd CAS*
Table A-1. 40 MHz DRAM Controller PLD Equation  (Sheet 12 of 19)

*Even address counter

state_diagram A3EVEN

state DEASSERT:
   if((CYCLE == IDLE) & A3) then ASSERT
else if((CYCLE == ACCESS4)) then ASSERT
else DEASSERT;

state ASSERT:
   if((CYCLE == IDLE) & !A3) then DEASSERT
else if((CYCLE == ACCESS4)) then DEASSERT
else ASSERT;

*Odd address counter

state_diagram A3ODD

state DEASSERT:
   if((CYCLE == IDLE) & A3) then ASSERT
else if((CYCLE == ACCESS5)) then ASSERT
else DEASSERT;

state ASSERT:
   if((CYCLE == IDLE) & !A3) then DEASSERT
else if((CYCLE == ACCESS5)) then DEASSERT
else ASSERT;

*Main DRAM state machine - ACCESS state machine

state_diagram CYCLE

state IDLE:
   if(ADS & !REFREQ & !ACC_PEND & DRAMADDR & SRASE) then ACCESS0
else if(ADS & !REFREQ & !ACC_PEND & DRAMADDR & !SRASE) then ACCESS1
else if(!REFREQ & ACC_PEND) then ACCESS0
else if(REFREQ) then REFRESH0
else IDLE;

state ACCESS0:
   goto ACCESS1;

state ACCESS1:
   if(W_R & !LA2) then ACCESS3
else if(!W_R & !LA2) then ACCESS4
else ACCESS2;

state ACCESS2:
   goto ACCESS3;
Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 13 of 19)
Table A-1. 40 MHz DRAM Controller PLD Equation

*Refresh Counter 1

state_diagram REFCT1

state Z0:
  if (!Q3 & (REFCT2 == Z0)) then Z0
  else
    Z15;

state Z1:
  if (Q3) then Z15
  else
    Z0;

state Z2:
  if (Q3) then Z15
  else
    Z1;

state Z3:
  if (Q3) then Z15
  else
    Z2;

state Z4:
  if (Q3) then Z15
  else
    Z3;

state Z5:
  if (Q3) then Z15
  else
    Z4;

state Z6:
  if (Q3) then Z15
  else
    Z5;

state Z7:
  if (Q3) then Z15
  else
    Z6;

state Z8:
  if (Q3) then Z15
  else
    Z7;

state Z9:
  if (Q3) then Z15
  else
    Z8;

state Z10:
  if (Q3) then Z15
  else
    Z9;
Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 15 of 19)

```
state Z11:
  if(Q3) then Z15
else
  Z10;
state Z12:
  if(Q3) then Z15
else
  Z11;
state Z13:
  if(Q3) then Z15
else
  Z12;
state Z14:
  if(Q3) then Z15
else
  Z13;
state Z15:
  if(Q3) then Z15
else
  Z14;
```
Table A-1. 40 MHz DRAM Controller PLD Equation  (Sheet 16 of 19)

*Refresh Counter 2

---

state_diagram REFCT2

state Z0:
  if(Q3) then Z15
  else
    Z0;

state Z1:
  if(Q3) then Z15
  else
    if(!Q3 & (REFCT1 == Z0)) then Z0;
    else
      Z1;

state Z2:
  if(Q3) then Z15
  else
    if(!Q3 & (REFCT1 == Z0)) then Z1;
    else
      Z2;

state Z3:
  if(Q3) then Z15
  else
    if(!Q3 & (REFCT1 == Z0)) then Z2;
    else
      Z3;

state Z4:
  if(Q3) then Z15
  else
    if(!Q3 & (REFCT1 == Z0)) then Z3;
    else
      Z4;

state Z5:
  if(Q3) then Z15
  else
    if(!Q3 & (REFCT1 == Z0)) then Z4;
    else
      Z5;

state Z6:
  if(Q3) then Z15
  else
    if(!Q3 & (REFCT1 == Z0)) then Z5;
    else
      Z6;

state Z7:
  if(Q3) then Z15
  else
    if(!Q3 & (REFCT1 == Z0)) then Z6;
    else
      Z7;
Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 17 of 19)

```plaintext
state Z8:
    if(Q3) then Z15
else
    if(!Q3 & (REFCT1 == Z0)) then Z7;
else
    Z8;
state Z9:
    if(Q3) then Z15
else
    if(!Q3 & (REFCT1 == Z0)) then Z8;
else
    Z9;
state Z10:
    if(Q3) then Z15
else
    if(!Q3 & (REFCT1 == Z0)) then Z9;
else
    Z10;
state Z11:
    if(Q3) then Z15
else
    if(!Q3 & (REFCT1 == Z0)) then Z10;
else
    Z11;
state Z12:
    if(Q3) then Z15
else
    if(!Q3 & (REFCT1 == Z0)) then Z11;
else
    Z12;
state Z13:
    if(Q3) then Z15
else
    if(!Q3 & (REFCT1 == Z0)) then Z12;
else
    Z13;
state Z14:
    if(Q3) then Z15
else
    if(!Q3 & (REFCT1 == Z0)) then Z13;
else
    Z14;
state Z15:
    if(Q3) then Z15
else
    if(!Q3 & (REFCT1 == Z0)) then Z14;
else
    Z15;
```
Equations

EQUATIONS

\[ Q3, Q2, Q1, Q0, !SEL_A, !SEL_B, !READY, !LA2, !ACC_PEND \].clk = CLK1;
\[ Q3..Q0 \].RE = RESET;

\[ !LA2, !ACC_PEND, !READY, !SEL_A, !SEL_B \].PR = RESET;

Indicates wait state cycles

\[ \text{WAIT} = (\text{CYCLE} == \text{ACCESS0}) \& \text{W_R} \]
\[ \# (\text{CYCLE} == \text{ACCESS1}) \& \text{W_R} \]
\[ \# (\text{CYCLE} == \text{ACCESS2}) \& \text{W_R} \]
\[ \# (\text{CYCLE} == \text{ACCESS3}) \& \text{W_R}; \]

\[ \text{REFREQ} = !T3 \& !T2 \& !T1 \& !T0 \& !S3 \& !S2 \& !S1 \& !S0; \]

Refresh required indicator

FLASH Chip Select

\[ \text{FLASHCS} := \text{ADS} \& \text{FLASHADDR} \& \text{!APK_ACTIVE} \]
\[ \# \!\text{ADS} \& \!\text{BLAST} \& \text{FLASHCS}; \]

FLASH OE control

\[ \text{FLASHRD} = \text{FLASHCS} \& \text{W_R}; \]

XCR OE control

\[ \text{XCROE} := \text{FLASHCS} \& \!\text{BLAST} \& \!\text{APK_ACTIVE} \]
\[ \# \!\text{ADS} \& \text{LEDADDR} \& !\text{BLAST}; \]

XCR DIR control

\[ \text{XCRDIR} = \text{W_R}; \]

Software reset indicator

\[ \text{SWRST} := \text{ADS} \& \text{SWRSTADDR} \]
\[ \# \!\text{ADS} \& \!\text{BLAST} \& \text{SWRST}; \]

Triggers the 7705

\[ \text{TRIGRST} := \text{TRIGRST}; \]
\[ \text{TRIGRST.RE} = \text{SWRST}; \]
<table>
<thead>
<tr>
<th>Table A-1. 40 MHz DRAM Controller PLD Equation (Sheet 19 of 19)</th>
</tr>
</thead>
</table>

```
"Pulse the HEX DISPLAY
"
LED_LAT := !ADS & LEDADDR & XCROE & !BLAST;
" Latched RASE or RASO
SRASE := RASE # RASO;
" DRAM data path control while reading
RDEN = !Q3 & W_R & RASE;
" Even DRAM data path control while writing
WRE = !Q3 & W_R & RASE;
" Odd DRAM data path control while writing
WRO = !Q3 & !W_R & RASE;
[[!FLASHCS,!XCROE,!SWRST,!TRIGRST,LED_LAT,SRASE].clk = CLK1;
[[!FLASHCS,!XCROE,!SWRST,!TRIGRST].pr = RESET;
LED_LAT.RE = RESET;
" Latched external reset
RESET := EXTRST;
RESET.CLK = CLK1;
" Test vectors
end CX40T
```
Table A-2. Signal and Product Term Allocation

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<thead>
<tr>
<th>OUTPUTS</th>
<th>BURIED MACROCELLS</th>
</tr>
</thead>
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<td>Product Terms</td>
</tr>
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<td>RASE</td>
<td>7</td>
</tr>
<tr>
<td>RASO</td>
<td>7</td>
</tr>
<tr>
<td>READY</td>
<td>6</td>
</tr>
<tr>
<td>A3E</td>
<td>3</td>
</tr>
<tr>
<td>A3O</td>
<td>3</td>
</tr>
<tr>
<td>SELA</td>
<td>4</td>
</tr>
<tr>
<td>MUX</td>
<td>1</td>
</tr>
<tr>
<td>RDEN</td>
<td>1</td>
</tr>
<tr>
<td>CASEB3</td>
<td>3</td>
</tr>
<tr>
<td>CASEB2</td>
<td>3</td>
</tr>
<tr>
<td>CASEB1</td>
<td>3</td>
</tr>
<tr>
<td>CASEB0</td>
<td>3</td>
</tr>
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</tr>
<tr>
<td>CASOB2</td>
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</tr>
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<tr>
<td>XCROE</td>
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<tr>
<td>XCRDIR</td>
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<tr>
<td>RESET</td>
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</tr>
<tr>
<td>WRE</td>
<td>1</td>
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<tr>
<td>WRO</td>
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</tr>
<tr>
<td>LED_LAT</td>
<td>1</td>
</tr>
<tr>
<td>SELB</td>
<td>4</td>
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