ADVANCE INFORMATION

Intel386™ EX EMBEDDED MICROPROCESSOR

- **Static Intel386™ CPU Core**
  - **— Low Power Consumption**
  - **— Operating Power Supply 2.7V to 5.5V**
  - **— Operating Frequency 16 MHz at 2.7V to 3.3V; 20 MHz at 3.0V to 3.6V; 25 MHz at 4.5V to 5.5V**
- **Transparent Power-management System Architecture**
  - **— Intel System Management Mode Architecture Extension for Truly Compatible Systems**
  - **— Power Management Transparent to Operating Systems and Application Programs**
  - **— Programmable Power-management Modes**
- **Powerdown Mode**
  - **— Clock Stopping at Any Time**
  - **— Only 10–20 µA Typical CPU Sink Current**
- **Full 32-bit Internal Architecture**
  - **— 8-, 16-, 32-bit Data Types**
  - **— 8 General Purpose 32-bit Registers**
- **Runs Intel386 Architecture Software in a Cost-effective 16-bit Hardware Environment**
  - **— Runs Same Applications and Operating Systems as the Intel386 SX and Intel386 DX Processors**
  - **— Object Code Compatible with 8086, 80186, 80286, and Intel386 Processors**
- **High-performance 16-bit Data Bus**
  - **— Two-clock Bus Cycles**
  - **— Address Pipelining Allows Use of Slower, Inexpensive Memories**
- **Integrated Memory Management Unit**
  - **— Virtual Memory Support**
  - **— Optional On-chip Paging**
  - **— 4 Levels of Hardware-enforced Protection**
  - **— MMU Fully Compatible with Those of the 80286 and Intel386 DX Processors**
- **Virtual 8086 Mode Allows Execution of 8086 Software in a Protected and Paged System**
- **Large Uniform Address Space**
  - **— 64 Megabyte Physical**
  - **— 64 Terabyte Virtual**
  - **— 4 Gigabyte Maximum Segment Size**
- **Numerics Support with Intel387™ SX and Intel387 SL Math Coprocessors**
- **On-chip Debugging Support Including Breakpoint Registers**
- **Complete System Development Support**
- **High Speed CHMOS Technology**
- **Two Package Types**
  - **— 132-pin Plastic Quad Flatpack**
  - **— 144-pin Thin Quad Flatpack**
- **Integrated Peripheral Functions**
  - **— Clock and Power Management Unit**
  - **— Chip-select Unit**
  - **— Interrupt Control Unit**
  - **— Timer Control Unit**
  - **— Watchdog Timer Unit**
  - **— Asynchronous Serial I/O Unit**
  - **— Synchronous Serial I/O Unit**
  - **— Parallel I/O Unit**
  - **— DMA and Bus Arbiter Unit**
  - **— Refresh Control Unit**
  - **— JTAG-compliant Test-logic Unit**

The Intel386™ EX Embedded Microprocessor is a highly integrated, 32-bit, fully static CPU optimized for embedded control applications. With a 16-bit external data bus, a 26-bit external address bus, and Intel's System Management Mode (SMM), the Intel386 EX microprocessor brings the vast software library of Intel386 architecture to embedded systems. It provides the performance benefits of 32-bit programming with the cost savings associated with 16-bit hardware systems.

September 1994 **Order Number:** 272420-004

Intel386™ EX EMBEDDED MICROPROCESSOR

CONTENTS

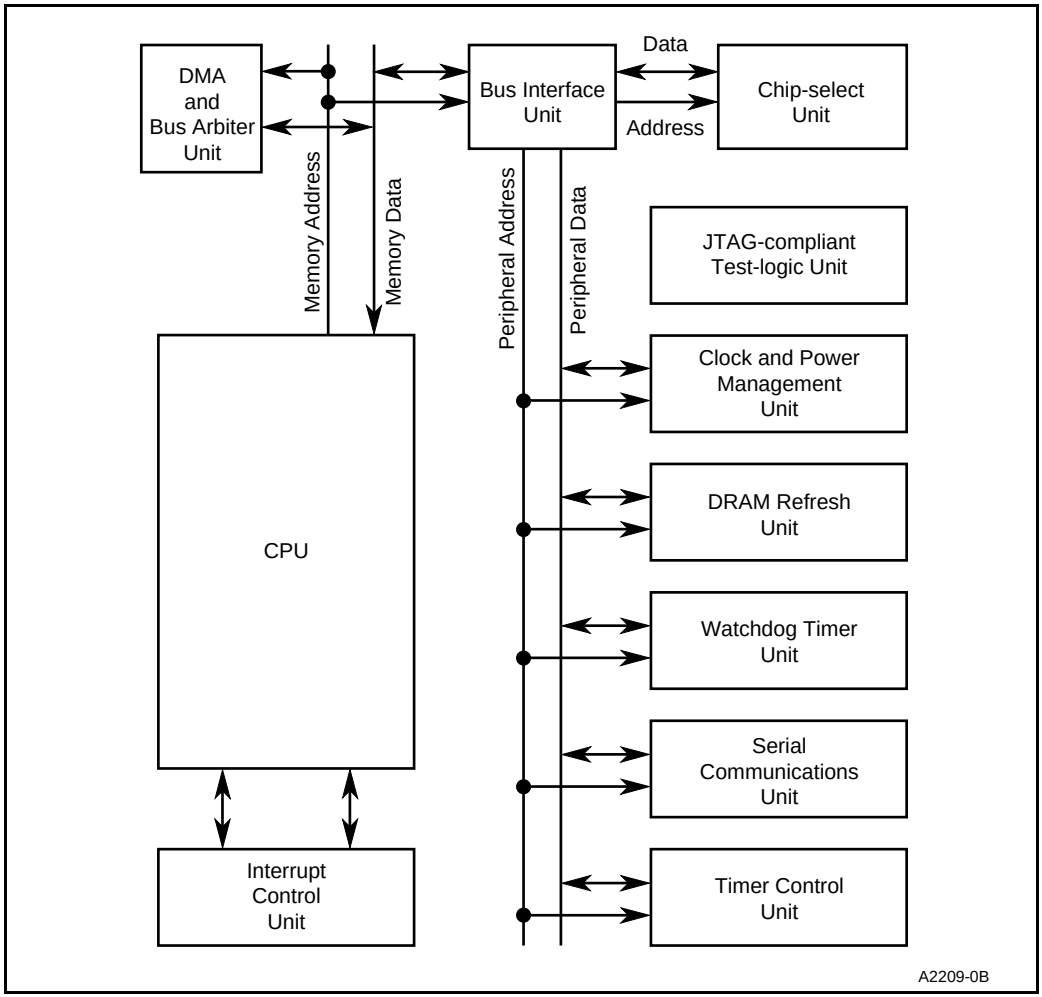

Figure 1. Intel386™ EX Microprocessor Block Diagram

1.0 PIN ASSIGNMENT

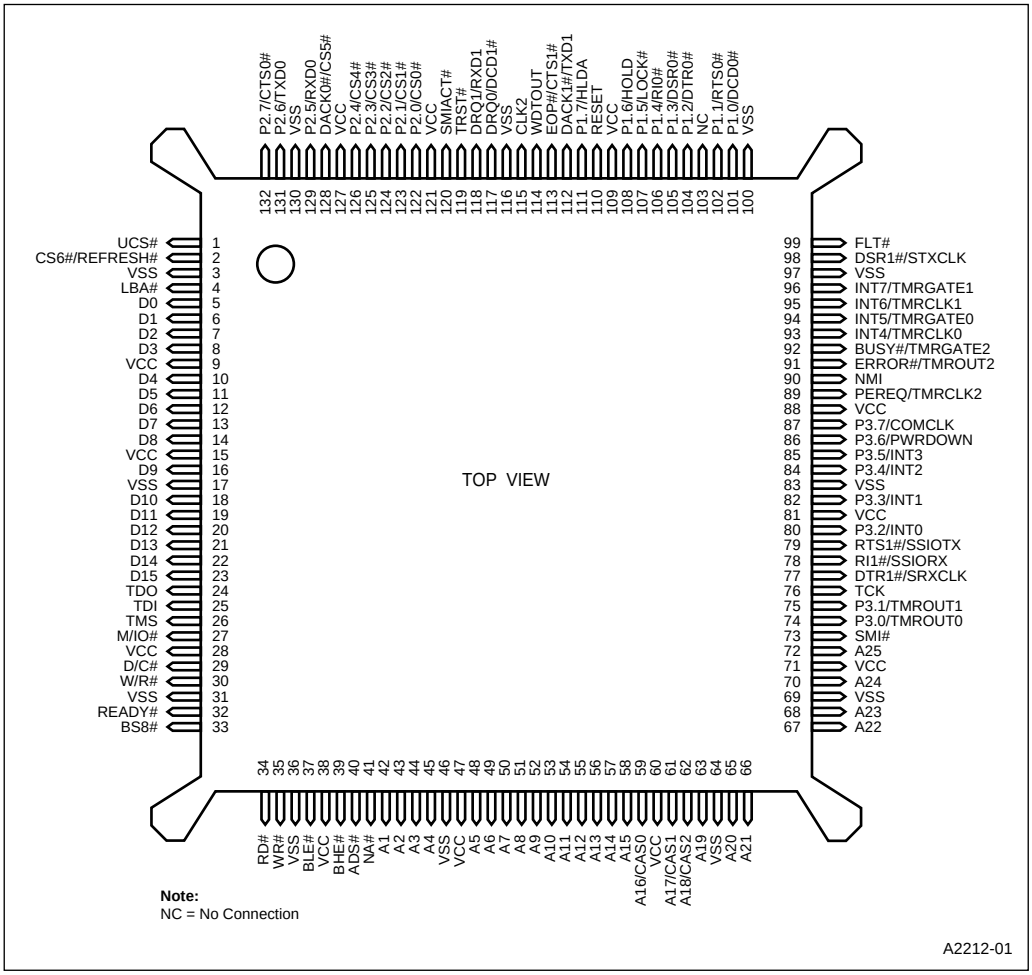

Figure 2. Intel386™ EX Microprocessor 132-Pin PQFP Pin Assignment

Table 1. 132-Pin PQFP Pin Assignment

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	UCS#	34	RD#	67	A22	100	V_{SS}
2	CS6#/REFRESH#	35	WR#	68	A23	101	P1.0/DCD0#
3	V_{SS}	36	V_{SS}	69	V_{SS}	102	P1.1/RTS0#
4	LBA#	37	BLE#	70	A24	103	NC
5	D0	38	V_{CC}	71	V_{CC}	104	P1.2/DTR0#
6	D1	39	BHE#	72	A25	105	P1.3/DSR0#
7	D2	40	ADS#	73	SMI#	106	P1.4/RI0#
8	D3	41	NA#	74	P3.0/TMROUT0	107	P1.5/LOCK#
9	V_{CC}	42	A1	75	P3.1/TMROUT1	108	P1.6/HOLD
10	D4	43	A2	76	TCK	109	V_{CC}
11	D5	44	A3	77	DTR1#/SRXCLK	110	RESET
12	D6	45	A4	78	RI1#/SSIORX	111	P1.7/HLDA
13	D7	46	V_{SS}	79	RTS1#/SSIOTX	112	DACK1#/TXD1
14	D8	47	V_{CC}	80	P3.2/INT0	113	EOP#/CTS1#
15	V_{CC}	48	A5	81	V_{CC}	114	WDTOUT
16	D9	49	A6	82	P3.3/INT1	115	CLK2
17	Vss	50	A7	83	V_{SS}	116	V_{SS}
18	D10	51	A8	84	P3.4/INT2	117	DRQ0/DCD1#
19	D11	52	A9	85	P3.5/INT3	118	DRQ1/RXD1
20	D12	53	A10	86	P3.6/PWRDOWN	119	TRST#
21	D13	54	A11	87	P3.7/COMCLK	120	SMIACT#
22	D14	55	A12	88	V_{CC}	121	V_{CC}
23	D15	56	A13	89	PEREQ/TMRCLK2	122	P2.0/CS0#
24	TDO	57	A14	90	NMI	123	P2.1/CS1#
25	TDI	58	A15	91	ERROR#/TMROUT2	124	P2.2/CS2#
26	TMS	59	A16/CAS0	92	BUSY#/TMRGATE2	125	P2.3/CS3#
27	M/IO#	60	V_{CC}	93	INT4/TMRCLK0	126	P2.4/CS4#
28	V_{CC}	61	A17/CAS1	94	INT5/TMRGATE0	127	V_{CC}
29	D/C#	62	A18/CAS2	95	INT6/TMRCLK1	128	DACK0#/CS5#
30	W/R#	63	A19	96	INT7/TMRGATE1	129	P2.5/RXD0
31	V_{SS}	64	V_{SS}	97	V_{SS}	130	V_{SS}
32	READY#	65	A20	98	DSR1#/STXCLK	131	P2.6/TXD0
33	BS8#	66	A21	99	FLT#	132	P2.7/CTS0#

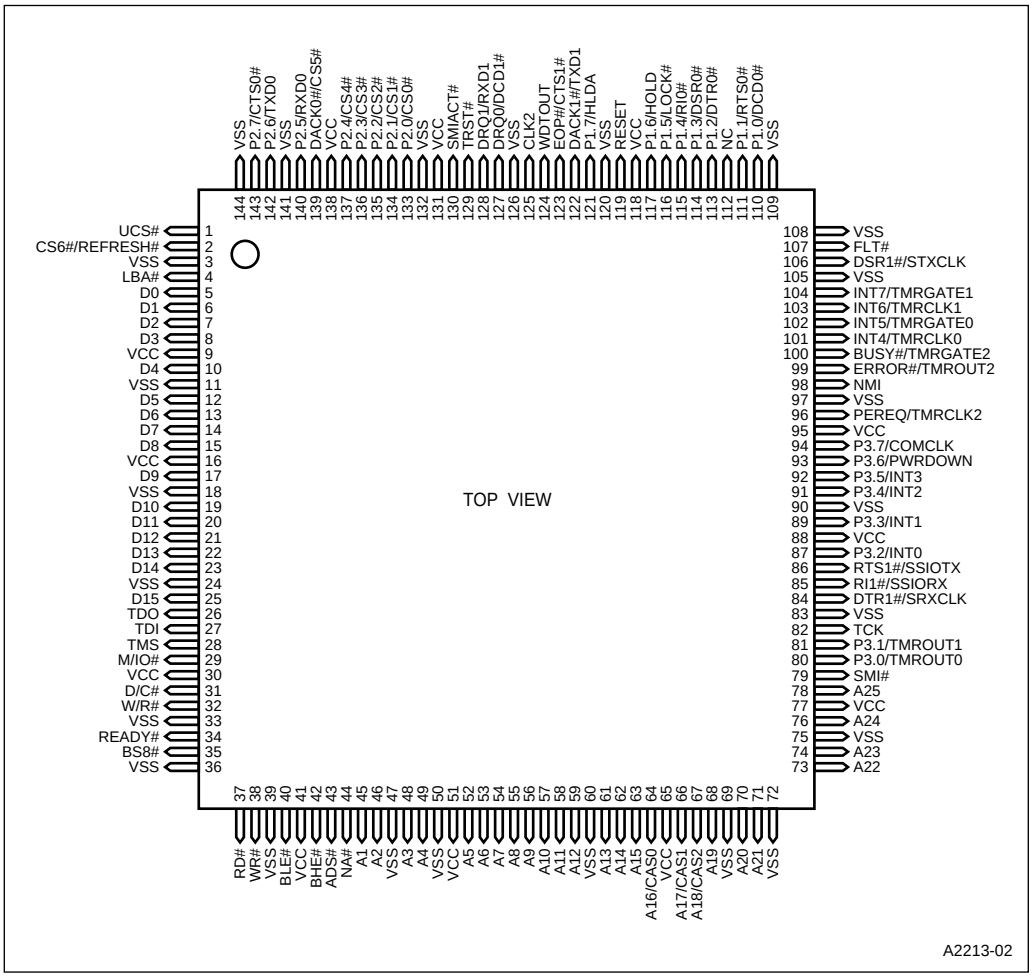

Figure 3. Intel386™ EX Microprocessor 144-Pin TQFP Pin Assignment

Table 2. 144 Pin TQFP Pin Assignment

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	UCS#	37	RD#	73	A22	109	V_{SS}
2	CS6#/REFRESH#	38	WR#	74	A23	110	P1.0/DCD0#
3	V_{SS}	39	V_{SS}	75	V_{SS}	111	P1.1/RTS0#
4	LBA#	40	BLE#	76	A24	112	NC
5	D0	41	V_{CC}	77	V_{CC}	113	P1.2/DTR0#
6	D1	42	BHE#	78	A25	114	P1.3/DSR0#
7	D2	43	ADS#	79	SMI#	115	P1.4/RI0#
8	D3	44	NA#	80	P3.0/TMROUT0	116	P1.5/LOCK#
9	V_{CC}	45	A1	81	P3.1/TMROUT1	117	P1.6/HOLD
10	D4	46	A2	82	TCK	118	V_{CC}
11	V_{SS}	47	V_{SS}	83	V_{SS}	119	RESET
12	D5	48	A3	84	DTR1#/SRXCLK	120	V_{SS}
13	D6	49	A4	85	RI1#/SSIORX	121	P1.7/HLDA
14	D7	50	V_{SS}	86	RTS1#/SSIOTX	122	DACK1#/TXD1
15	D8	51	V_{CC}	87	P3.2/INT0	123	EOP#/CTS1#
16	V_{CC}	52	A5	88	V_{CC}	124	WDTOUT
17	D9	53	A6	89	P3.3/INT1	125	CLK2
18	V_{SS}	54	A7	90	V_{SS}	126	V_{SS}
19	D10	55	A8	91	P3.4/INT2	127	DRQ0/DCD1#
20	D11	56	A9	92	P3.5/INT3	128	DRQ1/RXD1
21	D12	57	A10	93	P3.6/PWRDOWN	129	TRST#
22	D13	58	A11	94	P3.7/COMCLK	130	SMIACT#
23	D14	59	A12	95	V_{CC}	131	V_{CC}
24	V_{SS}	60	V_{SS}	96	PEREQ/TMRCLK2	132	V_{SS}
25	D15	61	A13	97	V_{SS}	133	P2.0/CS0#
26	TDO	62	A14	98	NMI	134	P2.1/CS1#
27	TDI	63	A15	99	ERROR#/TMROUT2	135	P2.2/CS2#
28	TMS	64	A16/CAS0	100	BUSY#/TMRGATE2	136	P2.3/CS3#
29	M/IO#	65	V_{CC}	101	INT4/TMRCLK0	137	P2.4/CS4#
30	V_{CC}	66	A17/CAS1	102	INT5/TMRGATE0	138	V_{CC}
31	D/C#	67	A18/CAS2	103	INT6/TMRCLK1	139	DACK0#/CS5#
32	W/R#	68	A19	104	INT7/TMRGATE1	140	P2.5/RXD0
33	V_{SS}	69	V_{SS}	105	V_{SS}	141	V_{SS}
34	READY#	70	A20	106	DSR1#/STXCLK	142	P2.6/TXD0
35	BS8#	71	A21	107	FLT#	143	P2.7/CTS0#
36	V_{SS}	72	V_{SS}	108	V_{SS}	144	V_{SS}

2.0 PIN DESCRIPTIONS

Table 3 lists the Intel386 EX microprocessor pin descriptions. The following definitions are used in the pin descriptions:

The named signal is active low.
I Standard CMOS input signal.
O Standard CMOS output signal.
I/O Input and output signal.
I/OD Input and open-drain output signal.
ST Schmitt-triggered input signal.
P Power pin.
G Ground pin.

Table 3. Intel386™ EX Microprocessor Pin Descriptions

Symbol	Type	Name and Function
A25:1	O	**Address Bus** outputs physical memory or port I/O addresses. These signals are valid when ADS# is active and remain valid until the next T1, T2P, or Ti. During HOLD cycles they are driven to a high-impedance state. A18:16 are multiplexed with CAS2:0.
ADS#	O	**Address Status** indicates that the processor is driving a valid bus-cycle definition and address (W/R#, D/C#, M/IO#, A25:1, BHE#, BLE#) onto its pins.
BHE#	O	**Byte High Enable** indicates that the processor is transferring a high data byte.
BLE#	O	**Byte Low Enable** indicates that the processor is transferring a low data byte.
BS8#	I	**Bus Size** indicates that an 8-bit device is currently being addressed.
BUSY#	I	**Busy** indicates that the math coprocessor is busy. If BUSY# is sampled low at the falling edge of RESET, the processor performs an internal self test. BUSY# is multiplexed with TMRGATE2.
CAS2:0	O	**Cascade Address** carries the slave address information from the 8259A master interrupt module during interrupt acknowledge bus cycles. CAS2:0 are multiplexed with A18:16.
CLK2	ST	**Clock Input** is connected to an external clock that provides the fundamental timing for the device.
COMCLK	I	**Serial Communications Baud Clock** is an alternate clock source for the asynchronous serial ports. COMCLK is multiplexed with P3.7.
CS6:0#	O	**Chip-selects** (lower) are activated when the address of a memory or I/O bus cycle is within the address region programmed by the user. They are multiplexed as follows: CS6# with REFRESH#, CS5# with DACK0#, and CS4:0# with P2.4:0.
CTS1:0#	I	**Clear to Send SIO1 and SIO0** prevent the transmission of data to the asynchronous serial port's RXD1 and RXD0 pins, respectively. CTS1# is multiplexed with EOP#, and CTS0# is multiplexed with P2.7. CTS1# requires an external pull-up resistor.
D15:0	I/O	**Data Bus** inputs data during memory read, I/O read, and interrupt acknowledge cycles and outputs data during memory and I/O write cycles. During writes, this bus is driven during phase 2 of T1 and remains active until phase 2 of the next T1, T1P, or Ti. During reads, data is latched on the falling edge of phase 2.

Table 3. Intel386™ EX Microprocessor Pin Descriptions (Continued)

Symbol	Type	Name and Function
DACK1:0#	O	**DMA Acknowledge 1 and 0** signal to an external device that the processor has acknowledged the corresponding DMA request and is relinquishing the bus. DACK1# is multiplexed with TXD1, and DACK0# is multiplexed with CS5#.
D/C#	O	**Data/Control** indicates whether the current bus cycle is a data cycle (memory or I/O read or write) or a control cycle (interrupt acknowledge, halt, or code fetch).
DCD1:0#	I	**Data Carrier Detect SIO1 and SIO0** indicate that the modem or data set has detected the corresponding asynchronous serial channel's data carrier. DCD1# is multiplexed with DRQ0, and DCD0# is multiplexed with P1.0.
DRQ1:0	I	**DMA External Request 1 and 0** indicate that a peripheral requires DMA service. DRQ1 is multiplexed with RXD1, and DRQ0 is multiplexed with DCD1#.
DSR1:0#	I	**Data Set Ready SIO1 and SIO0** indicate that the modem or data set is ready to establish a communication link with the corresponding asynchronous serial channel. DSR1# is multiplexed with STXCLK, and DSR0# is multiplexed with P1.3.
DTR1:0#	O	**Data Terminal Ready SIO1 and SIO0** indicate that the corresponding asynchronous serial channel is ready to establish a communication link with the modem or data set. DTR1# is multiplexed with SRXCLK, and DTR0# is multiplexed with P1.2.
EOP#	I/OD	**End of Process** indicates that the processor has reached terminal count during a DMA transfer. An external device can also pull this pin low. EOP# is multiplexed with CTS1#.
ERROR#	I	**Error** indicates that the math coprocessor has an error condition. ERROR# is multiplexed with TMROUT2.
FLT#	I	**Float** forces all bidirectional and output signals except TDO to a high-impedance state.
HLDA	O	**Bus Hold Acknowledge** indicates that the processor has surrendered control of its local bus to another bus master. HLDA is multiplexed with P1.7.
HOLD	I	**Bus Hold Request** allows another bus master to request control of the local bus. HLDA active indicates that bus control has been granted. HOLD is multiplexed with P1.6.
INT7:0	I	**Interrupt Requests** are maskable inputs that cause the CPU to suspend execution of the current program and then execute an interrupt acknowledge cycle. They are multiplexed as follows: INT7 with TMRGATE1, INT6 with TMRCLK1, INT5 with TMRGATE0, INT4 with TMRCLK0, and INT3:0 with P3.5:2.
LBA#	O	**Local Bus Access** is asserted whenever the processor provides the READY# signal to terminate a bus transaction. This occurs when an internal peripheral address is accessed or when the chip-select unit provides the READY# signal.
LOCK#	O	**Bus Lock** prevents other bus masters from gaining control of the system bus. LOCK# is multiplexed with P1.5.
M/IO#	O	**Memory/IO** Indicates whether the current bus cycle is a memory cycle or an I/O cycle. When M/IO# is high, the bus cycle is a memory cycle; when M/IO# is low, the bus cycle is an I/O cycle.
NA#	I	**Next Address** requests address pipelining.

Table 3. Intel386™ EX Microprocessor Pin Descriptions (Continued)

Symbol	Type	Name and Function
NMI	ST	**Nonmaskable Interrupt Request** is a non-maskable input that causes the CPU to suspend execution of the current program and execute an interrupt acknowledge cycle.
PEREQ	I	**Processor Extension Request** indicates that the math coprocessor has data to transfer to the processor. PEREQ is multiplexed with TMRCLK2.
P1.7:0	I/O	**Port 1, Pins 7:0** are multipurpose bidirectional port pins. They are multiplexed as follows: P1.7 with HLDA, P1.6 with HOLD, P1.5 with LOCK#, P1.4 with RI0#, P1.3 with DSR0#, P1.2 with DTR0#, P1.1 with RTS0#, and P1.0 with DCD0#.
P2.7:0	I/O	**Port 2, Pins 7:0** are multipurpose bidirectional port pins. They are multiplexed as follows: P2.7 with CTS0#, P2.6 with TXD0, P2.5 with RXD0, and P2.4:0 with CS4:0#.
P3.7:0	I/O	**Port 3, Pins 7:0** are multipurpose bidirectional port pins. They are multiplexed as follows: P3.7 with COMCLK, P3.6 with PWRDOWN, P3.5:2 with INT3:0, and P3.1:0 with TMROUT1:0.
PWRDOWN	O	**Powerdown** indicates that the processor is in powerdown mode. PWRDOWN is multiplexed with P3.6.
RD#	O	**Read Enable** indicates that the current bus cycle is a read cycle.
READY#	I/O	**Ready** indicates that the current bus transaction has completed. An external device or an internal signal can drive READY#. Internally, the chip-select wait-state logic can generate the ready signal and drive the READY# pin active.
RESET	ST	**Reset** suspends any operation in progress and places the processor into a known reset state.
REFRESH#	O	**Refresh** indicates that the current bus cycle is a refresh cycle. REFRESH# is multiplexed with CS6#.
RI1:0#	I	**Ring Indicator SIO1 and SIO0** indicate that the modem or data set has received a telephone ringing signal. RI1# is multiplexed with SSIORX, and RI0# is multiplexed with P1.4.
RTS1:0#	O	**Request-to-send SIO1 and SIO0** indicate that corresponding asynchronous serial channel is ready to exchange data with the modem or data set. RTS1# is multiplexed with SSIOTX, and RTS0# is multiplexed with P1.1.
RXD1:0	I	**Receive Data SIO1 and SIO0** accept serial data from the modem or data set to the corresponding asynchronous serial channel. RXD1 is multiplexed with DRQ1, and RXD0 is multiplexed with P2.5.
SMI#	ST	**System Management Interrupt** invokes System Management Mode (SMM). SMI# is the highest priority external interrupt. It is latched on its falling edge and it forces the CPU into SMM upon completion of the current instruction. SMI# is recognized on an instruction boundary and at each iteration for repeat string instructions. SMI# cannot interrupt LOCKed bus cycles or a currently executing SMM. If the processor receives a second SMI# while it is in SMM, it will latch the second SMI# on the SMI# falling edge. However, the processor must exit SMM by executing a resume instruction (RSM) before it can service the second SMI#.
SMIACT#	O	**System Management Interrupt Active** indicates that the processor is operating in System Management Mode (SMM). It is asserted when the processor initiates an SMM sequence and remains asserted (low) until the processor executes the resume instruction (RSM).

Table 3. Intel386™ EX Microprocessor Pin Descriptions (Continued)

Symbol	Type	Name and Function
SRXCLK	I/O	**SSIO Receive Clock** synchronizes data being accepted by the synchronous serial port. SRXCLK is multiplexed with DTR1#.
SSIORX	I	**SSIO Receive Serial Data** accepts serial data (most-significant bit first) being sent to the synchronous serial port. SSIORX is multiplexed with RI1#.
SSIOTX	O	**SSIO Transmit Serial Data** sends serial data (most-significant bit first) from the synchronous serial port. SSIOTX is multiplexed with RTS1#.
STXCLK	I/O	**SSIO Transmit Clock** synchronizes data being sent by the synchronous serial port. STXCLK is multiplexed with DSR1.
TCK	I	**TAP (Test Access Port) Controller Clock** provides the clock input for the JTAG logic.
TDI	I	**TAP (Test Access Port) Controller Data Input** is the serial input for test instructions and data.
TDO	O	**TAP (Test Access Port) Controller Data Output** is the serial output for test instructions and data.
TMRCLK2:0	I	**Timer/Counter Clock Inputs** can serve as external clock inputs for the corresponding timer/counters. (The timer/counters can also be clocked internally.) They are multiplexed as follows: TMRCLK2 with PEREQ, TMRCLK1 with INT6, and TMRCLK0 with INT4.
TMRGATE2:0	I	**Timer/Counter Gate Inputs** can control the corresponding timer/counter's counting (enable, disable, or trigger, depending on the programmed mode). They are multiplexed as follows: TMRGATE2 with BUSY#, TMRGATE1 with INT7, and TMRGATE0 with INT5.
TMROUT2:0	O	**Timer/Counter Outputs** provide the output of the corresponding timer/counter. The form of the output depends on the programmed mode. They are multiplexed as follows: TMROUT2 with ERROR#, TMROUT1 with P3.1, and TMROUT0 with P3.0.
TMS	I	**TAP (Test Access Port) Controller Mode Select** controls the sequence of the TAP controller's states.
TRST#	ST	**TAP (Test Access Port) Controller Reset** resets the TAP controller at power-up and each time it is activated.
TXD1:0	O	**Transmit Data SIO1 and SIO0** transmit serial data from the individual serial channels. TXD1 is multiplexed with DACK1#, and TXD0 is multiplexed with P2.6.
UCS#	O	**Upper Chip-select** is activated when the address of a memory or I/O bus cycle is within the address region programmed by the user.
V_{CC}	P	**System Power** provides the nominal DC supply input. Connected externally to a V_{CC} board plane.
V_{SS}	G	**System Ground** provides the 0V connection from which all inputs and outputs are measured. Connected externally to a ground board plane.
WDTOUT	O	**Watchdog Timer Output** indicates that the watchdog timer has expired.
W/R#	O	**Write/Read** indicates whether the current bus cycle is a write cycle or a read cycle. When W/R# is high, the bus cycle is a write cycle; when W/R# is low, the bus cycle is a read cycle.
WR#	O	**Write Enable** indicates that the current bus cycle is a write cycle.

3.0 FUNCTIONAL DESCRIPTION

The Intel386 EX microprocessor is a fully static, 32-bit processor optimized for embedded applications. It features low power and low voltage capabilities, integration of many commonly used DOS-type peripherals, and a 32-bit programming architecture compatible with the large software base of Intel386 processors. The following sections provide an overview of the integrated peripherals.

3.1 Clock Generation and Power Management Unit

The clock generation circuit includes a divide-by-two counter, a programmable divider for generating a prescaled clock (PSCLK), a divide-by-two counter for generating baud-rate clock inputs, and Reset circuitry. The CLK2 input provides the fundamental timing for the chip. It is divided by two internally to generate a 50% duty cycle Phase1 (PH1) and Phase 2 (PH2) for the core and integrated peripherals. For power management, separate clocks are routed to the core (PH1C/PH2C) and the peripheral modules (PH1P/PH2P).

Two Power Management modes are provided for flexible power-saving options. During Idle mode, the clocks to the CPU core are frozen in a known state (PH1C low and PH2C high), while the clocks to the peripherals continue to toggle. In Powerdown mode, the clocks to both core and peripherals are frozen in a known state (PH1C low and PH2C high). The Bus Interface Unit will not honor any DMA, DRAM refresh, or HOLD requests in Powerdown mode because the clocks to the entire device are frozen.

3.2 Chip-select Unit

The Chip-select Unit (CSU) decodes bus cycle address and status information and enables the appropriate chip-selects. The individual chip-selects become valid in the same bus state as the address and become inactive when either a new address is selected or the current bus cycle is complete.

The CSU is divided into eight separate chip-select regions, each of which can enable one of the eight chip-select pins. Each chip-select region can be mapped into memory or I/O space. A memory-mapped chip-select region can start on any $2^{(n+1)}$ Kbyte address location (where n = 0–15, depending upon the mask register). An I/O-mapped chip-select region can start on any $2^{(n+1)}$ byte address location (where n = 0–15, depending upon the mask register). The size of the region is also dependent upon the mask used.

3.3 Interrupt Control Unit

The Intel386 EX microprocessor's Interrupt Control Unit (ICU) contains two 8259A modules connected in a cascade mode. The 8259A modules make up the heart of the ICU. These modules are similar to the industry-standard 8259A architecture.

The Interrupt Control Unit directly supports up to eight external (INT7:0) and up to eight internal interrupt request signals. Pending interrupt requests are posted in the Interrupt Request Register, which contains one bit for each interrupt request signal. When an interrupt request is asserted, the corresponding Interrupt Request Register bit is set. The 8259A module can be programmed to recognize either an active-high level or a positive transition on the interrupt request lines. An internal Priority Resolver decides which pending interrupt request (if more than one exists) is the highest priority, based on the programmed operating mode. The Priority Resolver controls the single interrupt request line to the CPU. The Priority Resolver's default priority scheme places the master interrupt controller's IR0 as the highest priority and the master's IR7 as the lowest. The priority can be modified through software.

Besides the eight interrupt request inputs available to the Intel386 EX microprocessor, additional interrupts can be supported by cascaded external 8259A modules. Up to four external 8259A units can be cascaded to the master through connections to the INT3:0 pins. In this configuration, the interrupt acknowledge (INTA#) signal can be decoded externally using the ADS#, D/C#, W/R#, and M/IO# signals.

3.4 Timer Control Unit

The Timer Control Unit (TCU) on the Intel386 EX microprocessor has the same basic functionality as the industry-standard 82C54 counter/timer. The TCU

provides three independent 16-bit counters, each capable of handling clock inputs up to 8 MHz. This maximum frequency must be considered when programming the input clocks for the counters. Six programmable timer modes allow the counters to be used as event counters, elapsed-time indicators, programmable one-shots, and in many other applications. All modes are software programmable.

3.5 Watchdog Timer Unit

The Watchdog Timer (WDT) unit consists of a 32-bit down-counter that decrements every PH1P cycle, allowing up to 4.3 billion count intervals. The WDTOUT pin is driven high for sixteen CLK2 cycles when the down-counter reaches zero (the WDT times out). The WDTOUT signal can be used to reset the chip, to request an interrupt, or to indicate to the user that a ready-hang situation has occurred. The down-counter can also be updated with a user-defined 32-bit reload value under certain conditions. Alternatively, the WDT unit can be used as a bus monitor or as a general-purpose timer.

3.6 Asynchronous Serial I/O Unit

The Intel386 EX microprocessor's asynchronous Serial I/O (SIO) unit is a Universal Asynchronous Receiver/ Transmitter (UART). Functionally, it is equivalent to the National Semiconductor NS16450 and INS8250. The Intel386 EX microprocessor contains two full-duplex, asynchronous serial channels.

The SIO unit converts serial data characters received from a peripheral device or modem to parallel data and converts parallel data characters received from the CPU to serial data. The CPU can read the status of the serial port at any time during its operation. The status information includes the type and condition of the transfer operations being performed and any errors (parity, framing, overrun, or break interrupt).

Each asynchronous serial channel includes full modem control support (CTS#, RTS#, DSR#, DTR#, RI#, and DCD#) and is completely programmable. The programmable options include character length (5, 6, 7, or 8 bits), stop bits (1, 1.5, or 2), and parity (even, odd, forced, or none). In addition, it contains a programmable baud-rate generator capable of clock rates from 0 to 512 Kbaud.

3.7 Synchronous Serial I/O Unit

The Synchronous Serial I/O (SSIO) unit provides for simultaneous, bidirectional communications. It consists of a transmit channel, a receive channel, and a dedicated baud-rate generator. The transmit and receive channels can be operated independently (with different clocks) to provide non-lockstep, full-duplex communications; either channel can originate the clocking signal (Master Mode) or receive an externally generated clocking signal (Slave Mode).

The SSIO provides numerous features for ease and flexibility of operation. With a maximum clock input of 12.5 MHz to the baud-rate generator, the SSIO can deliver a baud rate of 5 Mbits per second. Each channel is double buffered. The two channels share the baud-rate generator and a multiply-by-two transmit and receive clock. The SSIO supports 16-bit serial communications with independently enabled transmit and receive functions and gated interrupt outputs to the interrupt controller.

3.8 Parallel I/O Unit

The Intel386 EX microprocessor has three 8-bit, general-purpose I/O ports. All port pins are bidirectional, with CMOS-level input and outputs. All pins have both a standard operating mode and a peripheral mode (a multiplexed function), and all have similar sets of control registers located in I/O address space. Ports 1 and 2 provide 8 mA of drive capability, while port 3 provides 16 mA.

3.9 DMA and Bus Arbiter Unit

The Intel386 EX microprocessor's DMA controller is a two-channel DMA; each channel operates independently of the other. Within the operation of the individual channels, several different data transfer modes are available. These modes can be combined in various configurations to provide a very versatile DMA controller. Its feature set has enhancements beyond the 8237 DMA family; however, it can be configured such that it can be used in an 8237-like

mode. Each channel can transfer data between any combination of memory and I/O with any combination (8 or 16 bits) of data path widths. An internal temporary register that can disassemble or assemble data to or from either an aligned or a nonaligned destination or source optimizes bus bandwidth

The bus arbiter, a part of the DMA controller, works much like the priority resolving circuitry of a DMA. It receives service requests from the two DMA channels, the external bus master, and the DRAM Refresh controller. The bus arbiter requests bus ownership from the core and resolves priority issues among all active requests when bus mastership is granted.

Each DMA channel consists of three major components: the Requestor, the Target, and the Byte Count. These components are identified by the contents of programmable registers that define the memory or I/O device being serviced by the DMA. The Requestor is the device that requires and requests service from the DMA controller. Only the Requestor is considered capable of initializing or terminating a DMA process. The Target is the device with which the Requestor wishes to communicate. The DMA process considers the Target a slave that is incapable of controlling the process. The Byte Count dictates the amount of data that must be transferred.

3.10 Refresh Control Unit

The Refresh Control Unit (RCU) simplifies dynamic memory controller design with its integrated address and clock counters. Integrating the RCU into the processor allows an external DRAM controller to use chip-selects, wait state logic, and status lines.

The Intel386 EX microprocessor's RCU consists of four basic functions. First, it provides a programmable-interval timer that keeps track of time. Second, it provides the bus arbitration logic to gain control of the bus to run refresh cycles. Third, it contains the logic to generate row addresses to refresh DRAM rows individually. And fourth, it contains the logic to signal the start of a refresh cycle.

Additionally, it contains a 13-bit address counter that forms the refresh address, supporting DRAMs with up to 13 rows of memory cells (13 refresh address bits). This includes all practical DRAM sizes for the Intel386 EX microprocessor's 64 Mbyte address space.

3.11 JTAG Test-logic Unit

The JTAG Test-logic Unit provides access to the device pins and to a number of other testable areas on the device. It is fully compliant with the IEEE 1149.1 standard and thus interfaces with five dedicated pins: TRST#, TCK, TMS, TDI, and TDO. It contains the Test Access Port (TAP) finite-state machine, a 4-bit instruction register, a 32-bit identification register, and a single-bit bypass register. The test-logic unit also contains the necessary logic to generate clock and control signals for the Boundary Scan chain.

Since the test-logic unit has its own clock and reset signals, it can operate autonomously. Thus, while the rest of the microprocessor is in Reset or Powerdown, the JTAG unit can read or write various register chains.

4.0 DESIGN CONSIDERATIONS

This section describes the Intel386 EX microprocessor's instruction set and its component and revision identifiers.

4.1 Instruction Set

The Intel386 EX microprocessor uses the same instruction set as the Intel386 SX microprocessor with the following exceptions.

The Intel386 EX microprocessor has one new instruction (RSM). This Resume instruction causes the processor to exit System Management Mode (SMM). RSM requires 338 clocks per instruction (CPI).

The Intel386 EX microprocessor requires more clock cycles than the Intel386 SX microprocessor to execute some instructions. Table 5 lists these instructions and the Intel386 EX microprocessor CPI. For

the equivalent Intel386 SX microprocessor CPI, refer to the “Instruction Set Clock Count Summary” table in the *Intel386™ SX Microprocessor* data sheet (order number 240187).

4.2 Component and Revision Identifiers

To assist users, the microprocessor holds a component identifier and revision identifier in its DX register after reset. The upper 8 bits of DX hold the component identifier, 23H. (The lower nibble, 3H, identifies the Intel386 architecture, while the upper nibble, 2H, identifies the second member of the Intel386 microprocessor family.)

The lower 8 bits of DX hold the revision level identifier. The revision identifier will, in general, chronologically track those component steppings that are intended to have certain improvements or distinction from previous steppings. The revision identifier will track that of the Intel386 CPU whenever possible. However, the revision identifier value is not guaranteed to change with every stepping revision or to follow a completely uniform numerical sequence, depending on the type or intent of the revision or the manufacturing materials required to be changed. Intel has sole discretion over these characteristics of the component. The initial revision identifier for the Intel386 EX microprocessor is 09H.

4.3. Package Thermal Specifications

The Intel386 EX microprocessor is specified for operation with case temperature (T_{CASE}) within the range of 0° C to 100° C. The case temperature can be measured in any environment to determine whether the microprocessor is within the specified operating range. The case temperature should be measured at the center of the top surface opposite the pins.

An increase in the ambient temperature (T_A) causes a proportional increase in the case temperature (T_{CASE}) and the junction temperature (T_J). A packaged device produces thermal resistance between junction and case temperatures (θ_{JC}) and between junction and ambient temperatures (θ_{JA}). The relationships between the temperature and thermal resistance parameters are expressed by these equations (P = power dissipated as heat = $V_{CC} \times I_{CC}$):

1. $T_J = T_{CASE} + P \times \theta_{JC}$
2. $T_A = T_J - P \times \theta_{JA}$
3. $T_{CASE} = T_A + P \times [\theta_{JA} - \theta_{JC}]$

A safe operating temperature can be calculated from equation 1 by using the maximum safe T_C of 100° C, the maximum power drawn by the chip in the specific design, and the θ_{JC} value from Table 4. The θ_{JA} value depends on the airflow (measured at the top of the chip) provided by the system ventilation. The θ_{JA} values are given for reference only and are not guaranteed.

Table 4. Thermal Resistances (0°C/W) θ_{JA}, θ_{JC}

Pkg	θ_{JC}	θ_{JA} versus Airflow (ft/min)		
		0	100	200
132 PQFP	6	41	36	32
144 TQFP	5	36	31	27

Figure 4 and Figure 5 provide examples of ambient temperature performance as a function of frequency. Each graph indicates a low, typical, and high power case for each package type. The high power case reflects high current consumption - i.e. many active peripherals, heavily loaded outputs, etc. The low power case reflects a condition similar to what would be seen with the device held in reset.

It should be noted that these graphs are only examples of thermal performance and not guaranteed values. Actual thermal performance may vary based on system design and should be calculated using actual power dissipation and the thermal resistance values given in Table 4.

Table 5. Intel386™ EX Microprocessor Clocks Per Instruction

Instruction	Clock Count		
	Virtual 8086 Mode (Note 1)	Real Address Mode or Virtual 8086 Mode	Protected Virtual Address Mode (Note 3)
POPA		28	35
IN: Fixed Port Variable Port	 27 28	 14 15	 7/29 8/29
OUT: Fixed Port Variable Port	 27 28	 14 15	 7/29 9/29
INS	30	17	9/32
OUTS	31	18	10/33
REP INS	31+6*n* (Note 2)	17+6*n* (Note 2)	10+6*n*/32+6*n* (Note 2)
REP OUTS	30+8*n* (Note 2)	16+8*n* (Note 2)	10+8*n*/31+8*n* (Note 2)
HLT		7	7
MOV C0, reg		10	10

NOTES:

1. The clock count values in this column apply if I/O permission allows I/O to the port in virtual 8086 mode. If the I/O bit map denies permission, exception fault 13 occurs; see clock counts for the INT 3 instruction in the "Instruction Set Clock Count Summary" table in the *Intel386™ SX Microprocessor* data sheet (order number 240187).
2. *n* = the number of times repeated.
3. When two clock counts are listed, the smaller value refers to a register operand and the larger value refers to a memory operand.

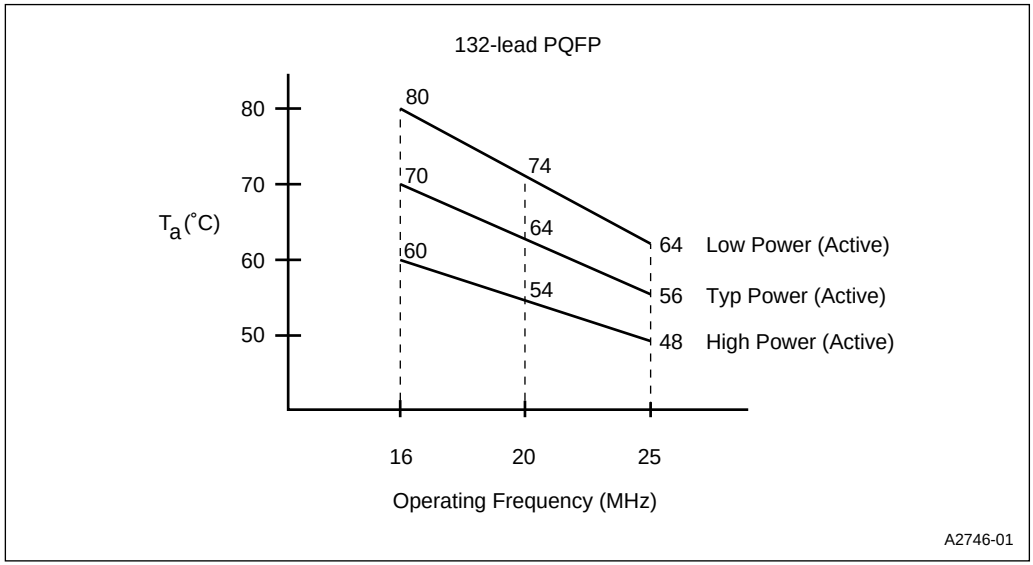

Figure 4. Ambient Temperature vs. Frequency for High, Low, and Typical Power Values (132-lead PQFP, V_{cc} = 5.0 V nominal)

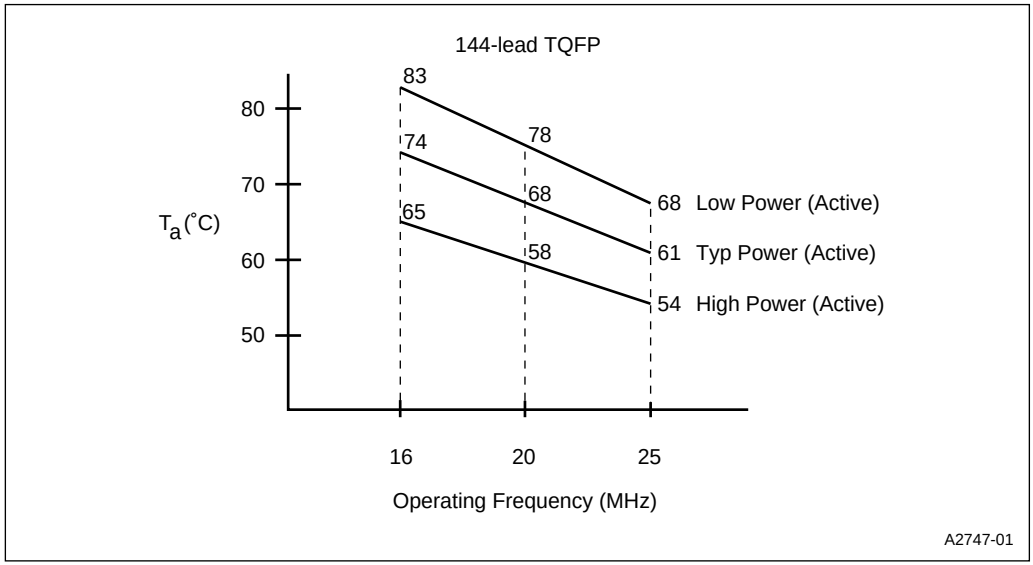

Figure 5. Ambient Temperature vs. Frequency for High, Low, and Typical Power Values (144-lead TQFP, V_{cc} = 5.0 V nominal)

5.0 DC SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Storage Temperature ..... –65°C to +150°C
Case Temperature Under Bias ..... –65°C to +110°C
Supply Voltage with Respect to V_{SS} ..... –0.5V to 6.5V
Voltage on Other Pins ..... –0.5V to V_{CC} + 0.5V

OPERATING CONDITIONS*

V_{CC} (Digital Supply Voltage) ..... 2.7V to 5.5 V
T_{CASE} (Case Temperature Under Bias) ..... 0°C to 100°C
F_{OSC} (Operating Frequency) ..... 0 MHz to 25 MHz

NOTICE: This document contains information on products in the sampling and initial production phases of development. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

**WARNING*: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Table 6. DC Characteristics

Symbol	Parameter	Min.	Max.	Unit	Test Condition
V_{IL}	Input Low Voltage	–0.5	$0.3V_{CC}$	V	
V_{IH}	Input High Voltage	$0.7V_{CC}$	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage All pins except Port 3 Port 3		 0.40 0.40	 V V	V_{CC} = 4.5V to 5.5V I_{OL} = 8 mA I_{OL} = 16 mA
V_{OL1}	Output Low Voltage All pins except Port 3 Port 3		 0.40 0.40	 V V	V_{CC} = 2.7V to 3.6V I_{OL} = 4 mA I_{OL} = 8 mA
V_{OH}	Output High Voltage All pins except Port 3 Port 3	 V_{CC}–0.8 V_{CC}–0.8		 V V	V_{CC} = 4.5V to 5.5V I_{OH} = –8 mA I_{OH} = –16 mA
V_{OH1}	Output High Voltage All pins except Port 3 Port 3	 V_{CC}–0.6 V_{CC}–0.6		 V V	V_{CC} = 2.7V to 3.6V I_{OH} = –4 mA I_{OH} = –8 mA
I_{LI}	Input Leakage Current		±15	µA	$0 \le V_{IN} \le V_{CC}$
I_{LO}	Output Leakage Current		±15	µA	$0.45V \le V_{OUT} \le V_{CC}$
I_{CC}	Supply Current		100 130 250	mA mA mA	16 MHz, 3.3V 20 MHz, 3.6V 25 MHz, 5.5V
I_{IDLE}	Idle Mode Current		35 45 85	mA mA mA	16 MHz, 3.3V 20 MHz, 3.6V 25 MHz, 5.5V
I_{PD}	Powerdown Current		100	µA	
C_S	Pin Capacitance (any pin to V_{SS})		10	pF	

6.0 AC SPECIFICATIONS

Table 7 lists output delays, input setup requirements, and input hold requirements. All AC specifications are relative to the CLK2 rising edge crossing the $V_{CC}/2$ level.

Figure 6 shows the measurement points for AC specifications. Inputs must be driven to the indicated voltage levels when AC specifications are measured. Output delays are specified with minimum and maximum limits measured as shown. The minimum delay times are hold times provided to external circuitry. Input setup and hold times are specified as minimums, defining the smallest acceptable sampling window. Within the sampling window, a synchronous input signal must be stable for correct operation.

Outputs ADS#, W/R#, CS5:0#, UCS#, D/C#, M/IO#, LOCK#, BHE#, BLE#, REFRESH#/CS6#, READY#, LBA#, A25:1, HLDA and SMIACT# change only at the beginning of phase one. D15:0 (write cycles) and PWRDOWN change only at the beginning of phase two. RD# and WR# change to their active states at the beginning of phase two, and to their inactive states (end of cycle) at the beginning of phase one.

The READY#, HOLD, BUSY#, ERROR#, PEREQ, BS8#, and D15:0 (read cycles) inputs are sampled at the beginning of phase one. The NA#, SMI#, and NMI inputs are sampled at the beginning of phase two.

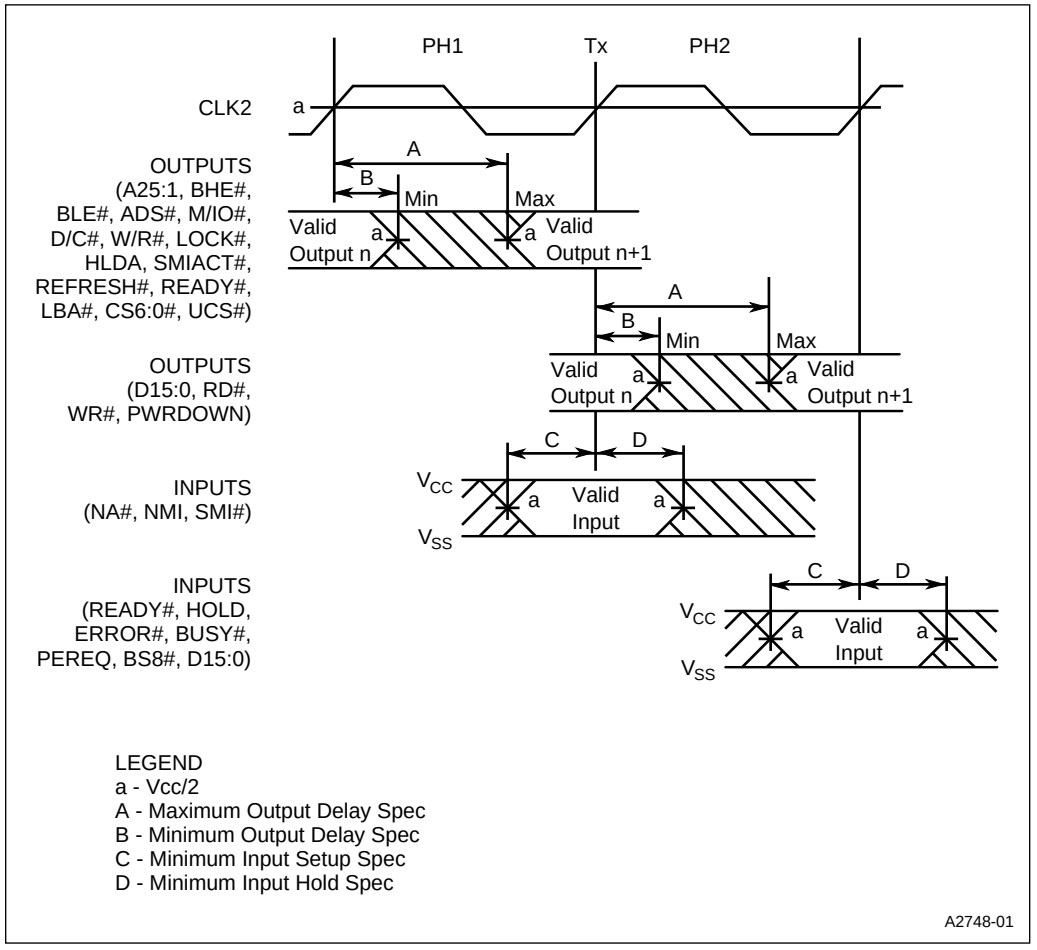

Figure 6. Drive Levels and Measurement Points for AC Specifications

Table 7. AC Characteristics

Symbol	Parameter	25 MHz 4.5V to 5.5V		20 MHz 3.0V to 3.6V		16 MHz 2.7V to 3.3V		Test Condition (Note 1)
		Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	
	Operating Frequency	0	25	0	20	0	16	one-half CLK2 frequency in MHz (Note 2)
t1	CLK2 Period	20		25		31		
t2a	CLK2 High Time	7		8		9		at $V_{CC}/2$ (Note 3)
t2b	CLK2 High Time	4		5		5		at V_{CC} – 0.8V for HV, at V_{CC} – 0.6V for LV (Note 3)
t3a	CLK2 Low Time	7		8		9		at $V_{CC}/2$ (Note 3)
t3b	CLK2 Low Time	5		6		7		at 0.8V (Note 3)
t4	CLK2 Fall Time		7		8		8	V_{CC} – 0.8V to 0.8V for HV, V_{CC} – 0.6V to 0.8V for LV (Note 3)
t5	CLK2 Rise Time		7		8		8	0.8V to V_{CC} –0.8V for HV, 0.8V to V_{CC} –0.6V for LV (Note 3)
t6	A25:1 Valid Delay	4	29	4	38	4	42	C_L = 50 pF (Note 4)
t7	A25:1 Float Delay	4	36	4	38	4	46	(Note 5)
t8	BHE#, BLE#, LOCK# Valid Delay	4	29	4	36	4	42	C_L = 50 pF (Note 4)

NOTES:
1. Throughout this table, HV refers to devices operating with V_{CC} = 4.5V to 5.5V. LV refers to devices operating with V_{CC} = 2.7V to 3.6V.
2. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
3. These are not tested. They are guaranteed by characterization.
4. Tested with C_L set at 50 pF. For LV devices, the t6 and t12 timings are guaranteed by design characterization with C_L set at 120 pF and all other Note 4 timings are guaranteed with C_L set at 75 pF.
5. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
6. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.
7. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.

Table 7. AC Characteristics (Continued)

Symbol	Parameter	25 MHz 4.5V to 5.5V		20 MHz 3.0V to 3.6V		16 MHz 2.7V to 3.3V		Test Condition (Note 1)
		Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	
t8a	SMIACT# Valid Delay	4	29	4	36	4	44	C_L = 50 pF (Note 4)
t9	BHE#, BLE#, LOCK# Float Delay	4	30	4	32	4	40	(Note 5)
t10	M/IO#, D/C#, W/R#, ADS#, REFRESH# Valid Delay	4	29	4	36	4	42	C_L = 50 pF (Note 4)
t10a	RD#, WR# Valid Delay	4	29	4	36	4	42	
t11	M/IO#, D/C#, W/R#, REFRESH#, ADS# Float Delay	4	39	4	39	4	44	(Note 5)
t12	D15:0 Write Data Valid Delay	4	31	4	40	4	44	C_L = 50 pF (Note 4)
t13	D15:0 Write Data Float delay	4	24	4	29	4	37	(Note 5)
t14	HLDA Valid Delay	4	27	4	36	4	41	C_L = 50 pF (Note 4)
t15	NA# Setup Time	5		7		9		
t16	NA# Hold Time	10		13		15		
t19	READY# Setup Time	9		12		19		
t19a	BS8# Setup Time	11		17		19		
t20	READY#, BS8# Hold Time	4		4		4		
t21	D15:0 Read Setup Time	7		9		9		
t22	D15:0 Read Hold Time	5		6		6		

NOTES:
1. Throughout this table, HV refers to devices operating with V_{CC} = 4.5V to 5.5V. LV refers to devices operating with V_{CC} = 2.7V to 3.6V.
2. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
3. These are not tested. They are guaranteed by characterization.
4. Tested with C_L set at 50 pF. For LV devices, the t6 and t12 timings are guaranteed by design characterization with C_L set at 120 pF and all other Note 4 timings are guaranteed with C_L set at 75 pF.
5. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
6. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.
7. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.

Table 7. AC Characteristics (Continued)

Symbol	Parameter	25 MHz 4.5V to 5.5V		20 MHz 3.0V to 3.6V		16 MHz 2.7V to 3.3V		Test Condition (Note 1)
		Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	
t23	HOLD Setup Time	9		17		26		
t24	HOLD Hold Time	3		5		5		
t25	RESET Setup Time	8		12		13		
t26	RESET Hold Time	4		4		4		
t27	NMI Setup Time	12		16		18		(Note 6)
t27a	SMI# Setup Time	12		16		18		(Note 6)
t28	NMI Hold Time	6		16		16		(Note 6)
t28a	SMI# Hold Time	6		16		16		(Note 6)
t29	PEREQ, ERROR#, BUSY# Setup Time	6		14		16		(Note 6)
t30	PEREQ, ERROR#, BUSY# Hold Time	5		5		5		(Note 6)
t31	READY# Valid Delay	4	36	4	44	4	52	
t32	READY# Float Delay	4	34	4	42	4	50	
t33	LBA# Valid Delay	4	32	4	40	4	48	
t34	CS6:0#, UCS# Valid Delay	4	39	4	48	4	54	
t41	A25:1, BHE#, BLE# Valid to WR# Low	0		0		0		
t41a	UCS#, CS6:0# Valid to WR# Low	0		0		0		
t42	A25:1, BHE#, BLE# Hold After WR# High	5		5		5		

NOTES:
1. Throughout this table, HV refers to devices operating with V_{CC} = 4.5V to 5.5V. LV refers to devices operating with V_{CC} = 2.7V to 3.6V.
2. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
3. These are not tested. They are guaranteed by characterization.
4. Tested with C_L set at 50 pF. For LV devices, the t6 and t12 timings are guaranteed by design characterization with C_L set at 120 pF and all other Note 4 timings are guaranteed with C_L set at 75 pF.
5. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
6. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.
7. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.

Table 7. AC Characteristics (Continued)

Symbol	Parameter	25 MHz 4.5V to 5.5V		20 MHz 3.0V to 3.6V		16 MHz 2.7V to 3.3V		Test Condition (Note 1)
		Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	
t42a	UCS#, CS6:0# Hold after WR# High	5		5		5		
t43	D15:0 Output Valid to WR# High	3CLK2 –27		3CLK2 – 36		3CLK2 – 40		(Note 7)
t44	D15:0 Output Hold After WR# High	CLK2 –10		CLK2 –10		CLK2 –10		
t45	WR# High to D15:0 Float		CLK2 + 10		CLK2 + 10		CLK2 +10	(Note 5)
t46	WR# Pulse Width	3CLK2 –15		3CLK2 –15		3CLK2 –15		
t47	A25:1, BHE#, BLE# Valid to D15:0 Valid		4CLK2 - 36		4CLK2 - 47		4CLK2 - 51	(Note 7)
t47a	UCS#, CS6:0# Valid to D15-D0 Valid		4CLK2 - 46		4CLK2 - 57		4CLK2 - 61	(Note 7)
t48	RD# Low to D15:0 Input Valid		3CLK2 – 36		3CLK2 – 45		3CLK2 – 51	(Note 7)
t49	D15:0 Hold After RD# High	2		2		2		
t50	RD# High to D15:0 Float		10		15		18	(Note 5)
t51	A25:1, BHE#, BLE# Hold After RD# High	0		0		0		
t51a	UCS#, CS6:0# Hold after RD# High	0		0		0		
t52	RD# Pulse Width	3CLK2 –15		3CLK2 –15		3CLK2 –15		

NOTES:
1. Throughout this table, HV refers to devices operating with V_{CC} = 4.5V to 5.5V. LV refers to devices operating with V_{CC} = 2.7V to 3.6V.
2. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
3. These are not tested. They are guaranteed by characterization.
4. Tested with C_L set at 50 pF. For LV devices, the t6 and t12 timings are guaranteed by design characterization with C_L set at 120 pF and all other Note 4 timings are guaranteed with C_L set at 75 pF.
5. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
6. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.
7. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.

Table 7. AC Characteristics (Continued)

Symbol	Parameter	25 MHz 4.5V to 5.5V		20 MHz 3.0V to 3.6V		16 MHz 2.7V to 3.3V		Test Condition (Note 1)
		Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	
Synchronous Serial I/O (SSIO) Unit								
t100	STXCLK, SRXCLK Frequency (Master Mode)		CLK2/8		CLK2/8		CLK2/8	(Unit is MHz)
t101	STXCLK, SRXCLK Frequency (Slave Mode)		CLK2/4		CLK2/4		CLK2/4	(Unit is MHz; CLK2/4 or 6.25 MHZ, whichever is less)
t102	STXCLK, SRXCLK Low Time	3CLK2/2		3CLK2/2		3CLK2/2		
t103	STXCLK, SRXCLK High Time	3CLK2/2		3CLK2/2		3CLK2/2		
t104	STXCLK Low to SSIOTX Delay		10		15		18	
t105	SSIORX to SRXCLK High Setup Time	10		15		18		
t106	SSIORX from SRXCLK Hold Time	10		15		18		
Timer Control Unit (TCU) Inputs								
t107	TMRCLK*n* Frequency		8		8		8	(Unit is MHz)
t108	TMRCLK*n* Low	60		60		60		
t109	TMRCLK*n* High	60		60		60		
t110	TMRGATE*n* High Width	50		50		60		
t111	TMRGATE*n* Low Width	50		50		60		

NOTES:
1. Throughout this table, HV refers to devices operating with V_{CC} = 4.5V to 5.5V. LV refers to devices operating with V_{CC} = 2.7V to 3.6V.
2. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
3. These are not tested. They are guaranteed by characterization.
4. Tested with C_L set at 50 pF. For LV devices, the t6 and t12 timings are guaranteed by design characterization with C_L set at 120 pF and all other Note 4 timings are guaranteed with C_L set at 75 pF.
5. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
6. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.
7. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.

Table 7. AC Characteristics (Continued)

Symbol	Parameter	25 MHz 4.5V to 5.5V		20 MHz 3.0V to 3.6V		16 MHz 2.7V to 3.3V		Test Condition (Note 1)
		Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	
t112	TMRGATE*n* to TMRCLK Setup Time (external TMRCLK only)	10		15		18		
Timer Control Unit (TCU) Outputs								
t113	TMRGATE*n* Low to TMROUT Valid		36		48		52	
t114	TMRCLK*n* Low to TMROUT Valid		36		48		52	
Interrupt Control Unit (ICU) Inputs								
t115	D7:0 Setup Time (INTA# Cycle 2)	7		9		9		
t116	D7:0 Hold Time (INTA# Cycle 2)	5		6		6		
Interrupt Control Unit (ICU) Outputs								
t117	CLK2 High to CAS2:0 Valid		34		48		54	
DMA Unit Inputs								
t118	DREQ Setup Time (Sync Mode)	17		19		21		
t119	DREQ Hold Time (Sync Mode)	4		4		4		
t120	DREQ Setup Time (Async Mode)	10		11		11		
t121	DREQ Hold Time (Async Mode)	10		11		11		

NOTES:

1. Throughout this table, HV refers to devices operating with V_{CC} = 4.5V to 5.5V. LV refers to devices operating with V_{CC} = 2.7V to 3.6V.
2. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
3. These are not tested. They are guaranteed by characterization.
4. Tested with C_L set at 50 pF. For LV devices, the t6 and t12 timings are guaranteed by design characterization with C_L set at 120 pF and all other Note 4 timings are guaranteed with C_L set at 75 pF.
5. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
6. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.
7. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.

Table 7. AC Characteristics (Continued)

Symbol	Parameter	25 MHz 4.5V to 5.5V		20 MHz 3.0V to 3.6V		16 MHz 2.7V to 3.3V		Test Condition (Note 1)
		Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	Min. (ns)	Max. (ns)	
t122	EOP# Setup Time (Sync Mode)	13		17		21		
t123	EOP# Hold Time (Sync Mode)	4		4		4		
t124	EOP# Setup Time (Async Mode)	10		11		11		
t125	EOP# Hold Time (Async Mode)	11		11		11		
DMA Unit Outputs								
t126	DACK# Output Valid Delay	4	29	4	36	4	42	
t127	EOP# Active Delay	4	30	4	40	4	46	
t128	EOP# Float Delay	4	33	4	41	4	49	(Note 5)
JTAG Test-logic Unit								
t129	TCK Frequency		10		10		10	(Unit is MHz)

NOTES:
1. Throughout this table, HV refers to devices operating with V_{CC} = 4.5V to 5.5V. LV refers to devices operating with V_{CC} = 2.7V to 3.6V.
2. Tested at maximum operating frequency and guaranteed by design characterization at lower operating frequencies.
3. These are not tested. They are guaranteed by characterization.
4. Tested with C_L set at 50 pF. For LV devices, the t6 and t12 timings are guaranteed by design characterization with C_L set at 120 pF and all other Note 4 timings are guaranteed with C_L set at 75 pF.
5. Float condition occurs when maximum output current becomes less than I_{LO} in magnitude. Float delay is not fully tested.
6. These inputs may be asynchronous to CLK2. The setup and hold specifications are given for testing purposes to ensure recognition within a specific CLK2 period.
7. These specifications are for information only and are not tested. They are intended to assist the designer in selecting memory speeds. For each wait state in the design add two CLK2 cycles to the specification.

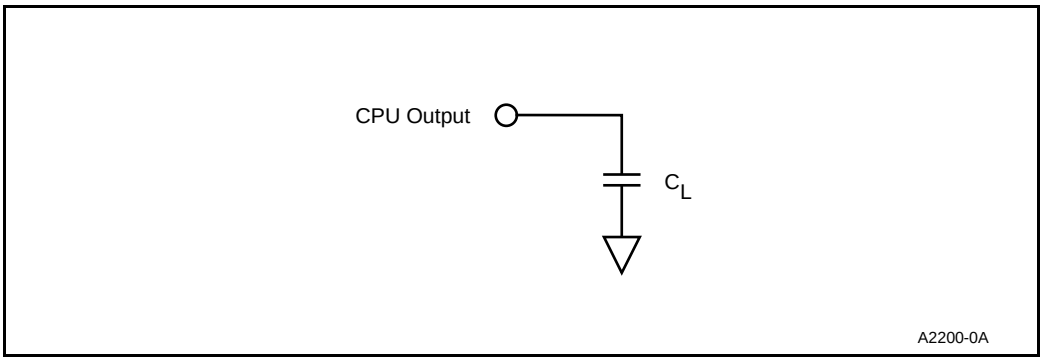

Figure 7. AC Test Loads

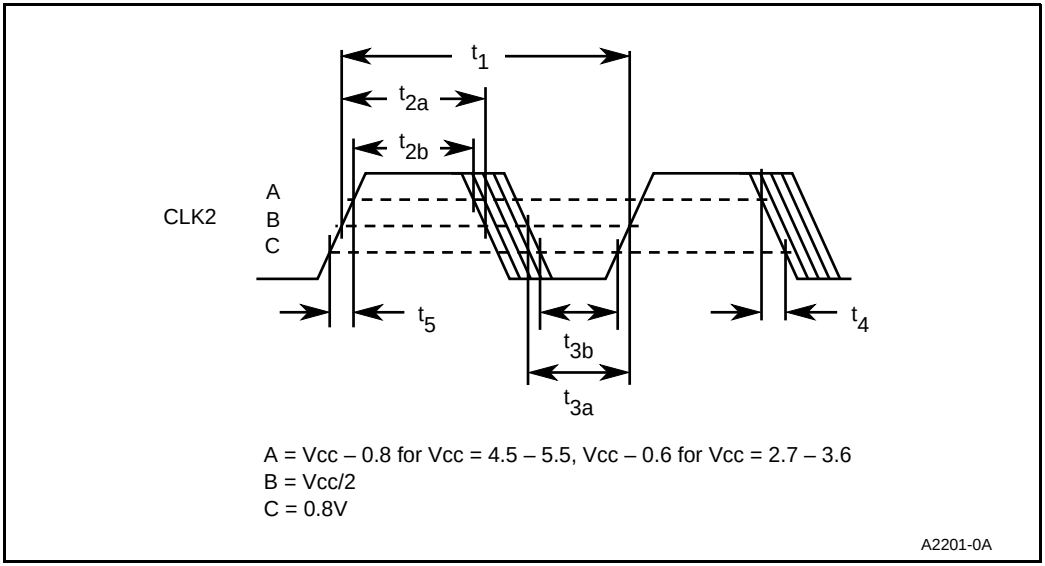

Figure 8. CLK2 Waveform

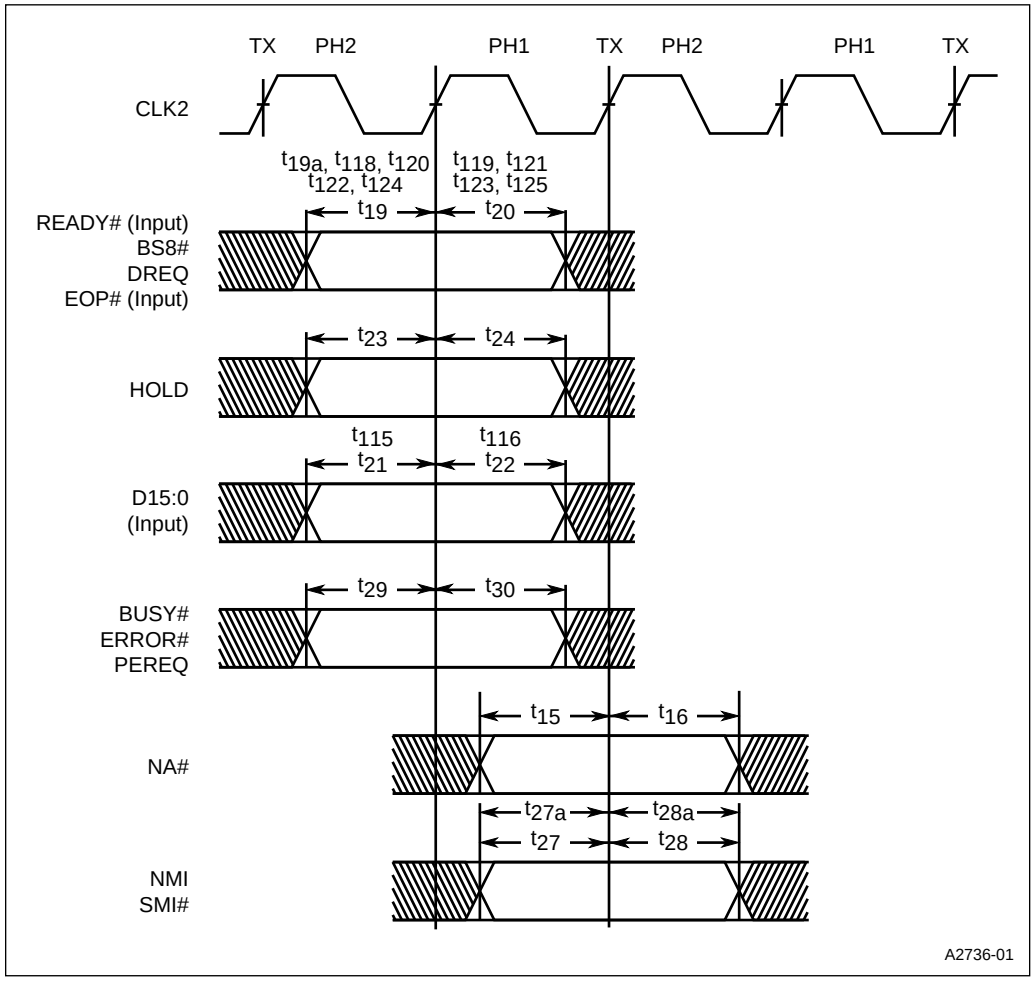

Figure 9. AC Timing Waveforms — Input Setup and Hold Timing

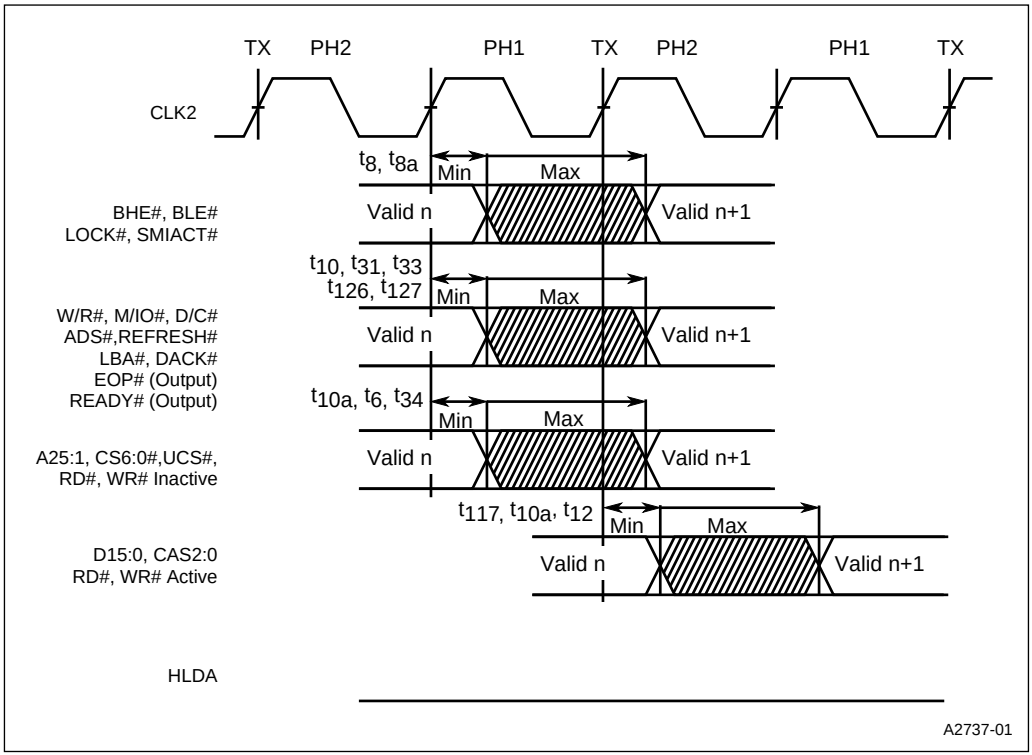

Figure 10. AC Timing Waveforms — Output Valid Delay Timing

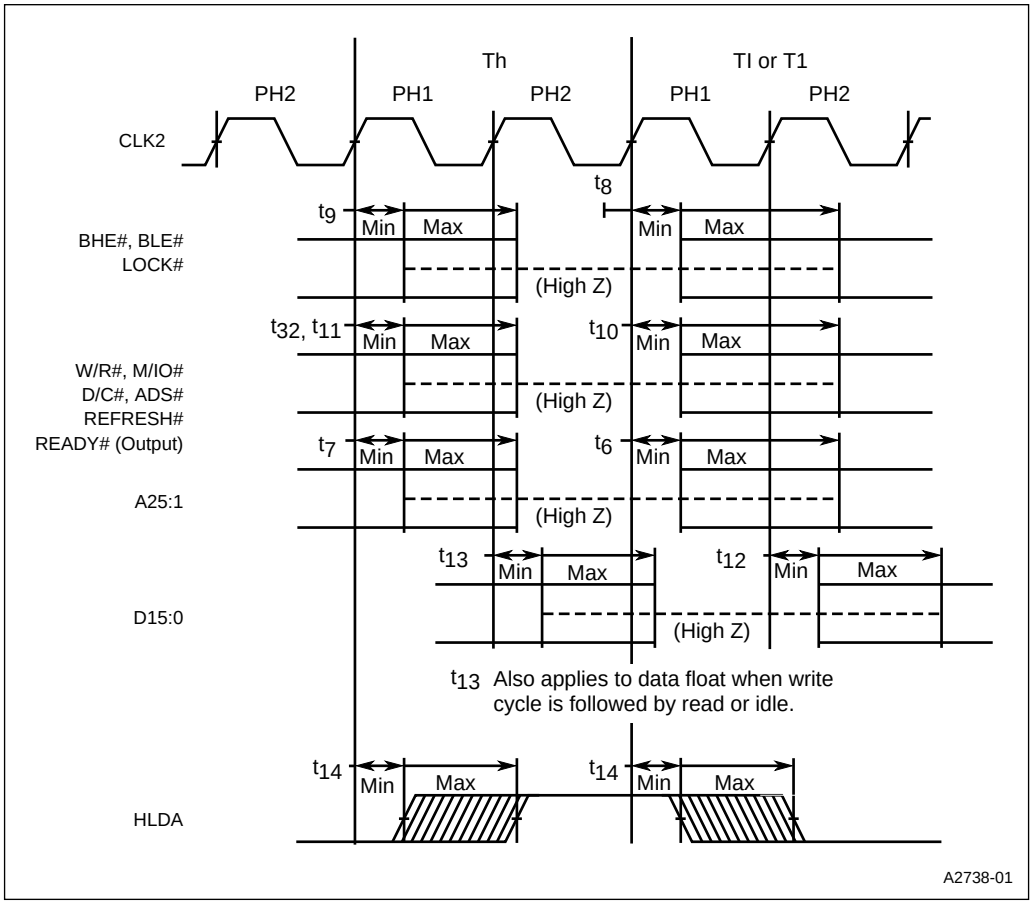

Figure 11. AC Timing Waveforms — Output Float Delay and HLDA Valid Delay Timing

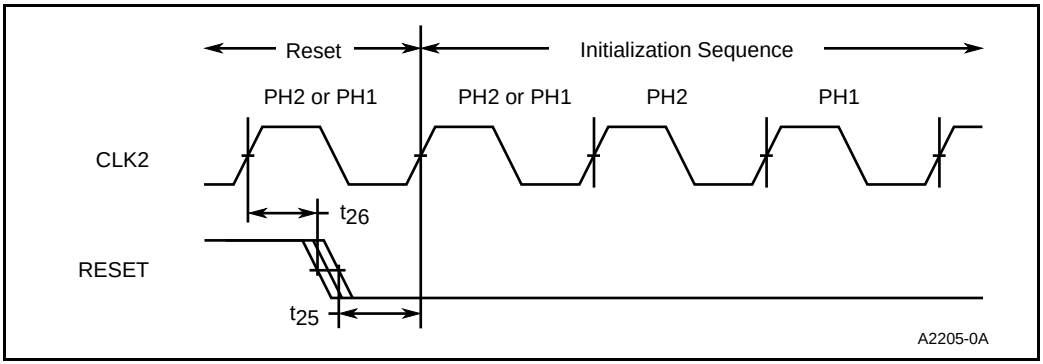

Figure 12. AC Timing Waveforms — RESET Setup and Hold Timing and Internal Phase

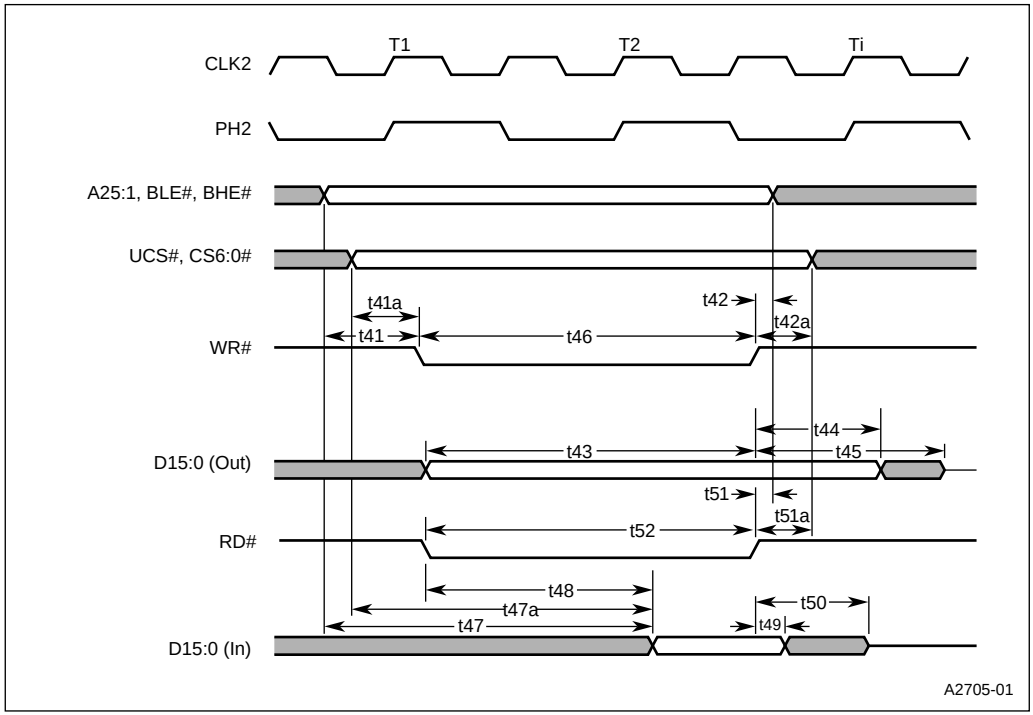

Figure 13. AC Timing Waveforms — Relative Signal Timing

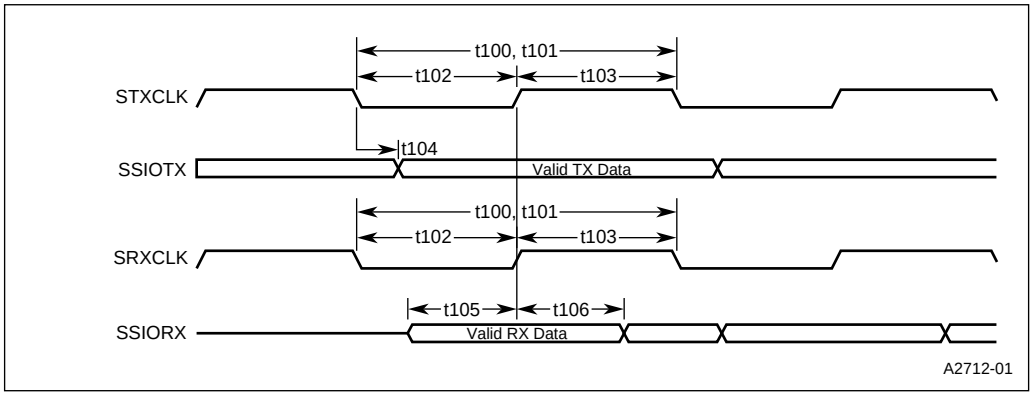

Figure 14. AC Timing Waveforms — SSIO Timing

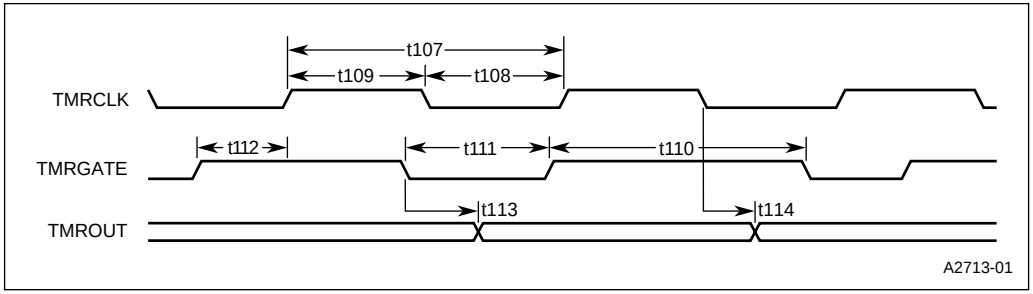

Figure 15. AC Timing Waveforms — Timer/Counter Timing

7.0 BUS CYCLE WAVEFORMS

Figures 16 through 24 present various bus cycles that are generated by the processor. What is shown in the figure is the relationship of the various bus signals to CLK2. These figures along with the information present in AC Specifications allow the user to determine critical timing analysis for a given application

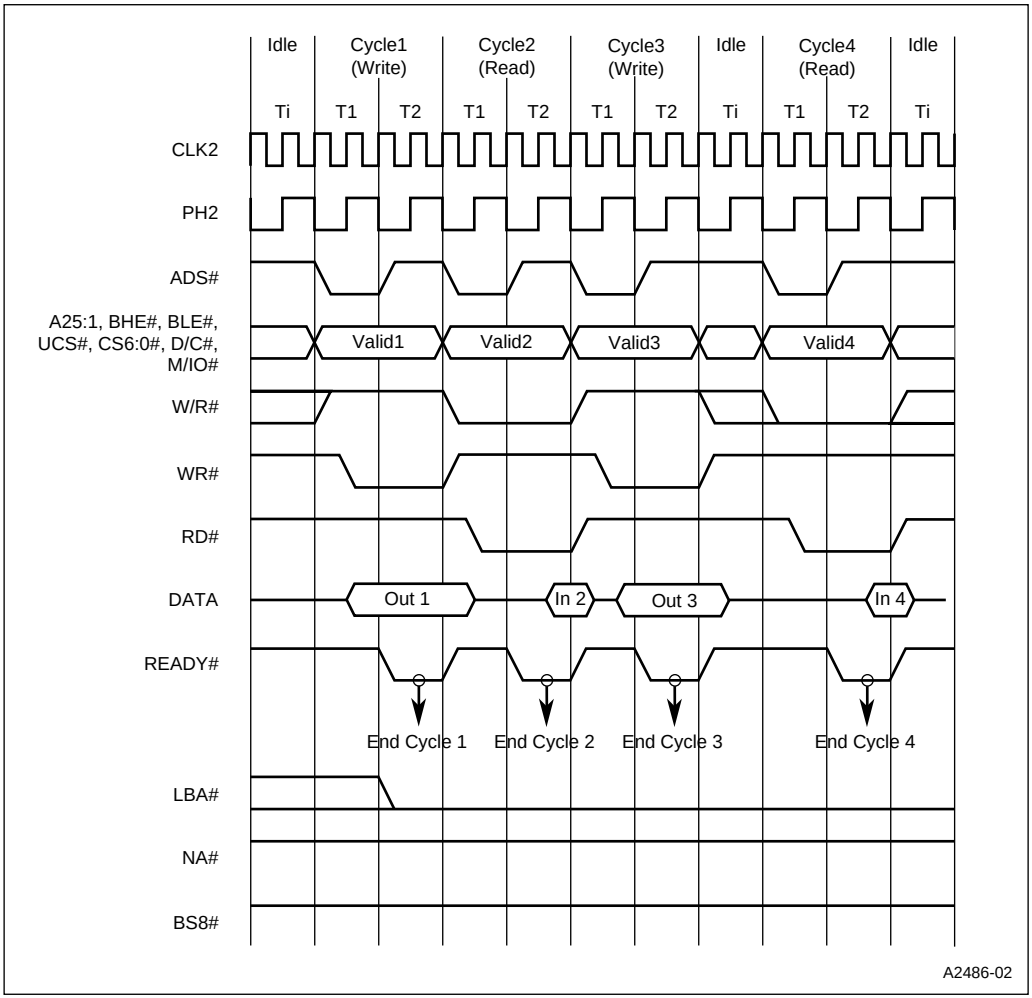

Figure 16. Local Bus Read and Write Cycles (Zero Wait States)

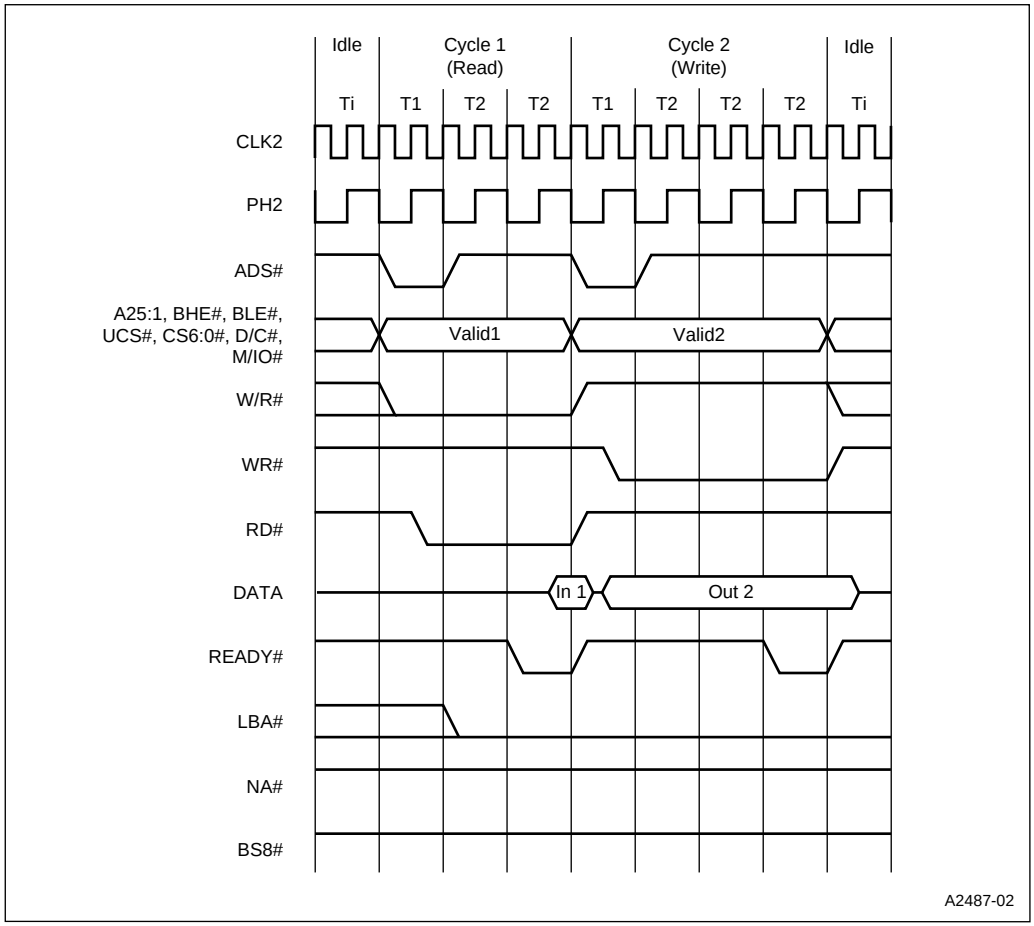

Figure 17. Local Bus Read and Write Cycles (With Wait States)

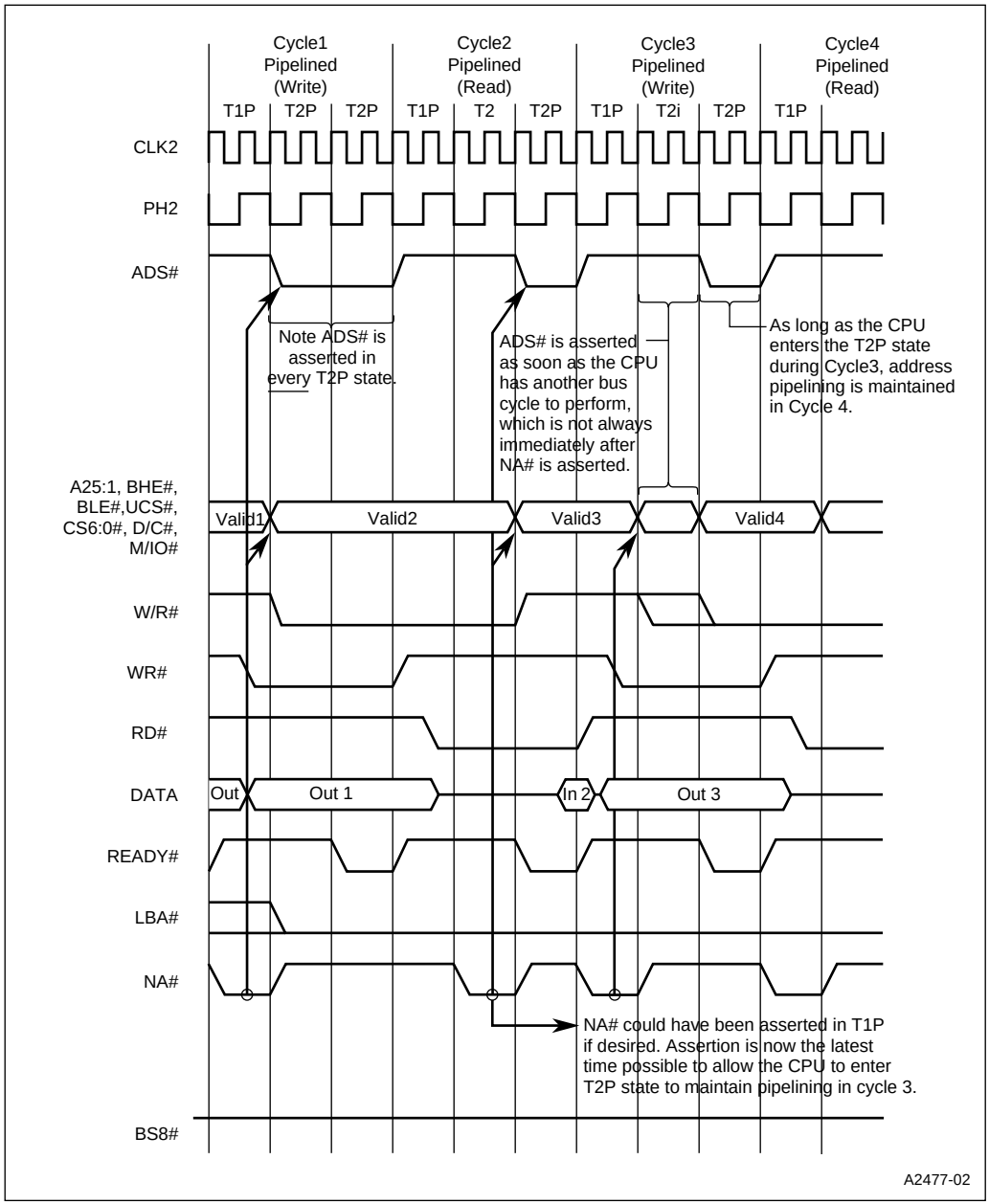

Figure 18. Pipelined Local Bus Read and Write Cycles (With Wait States)

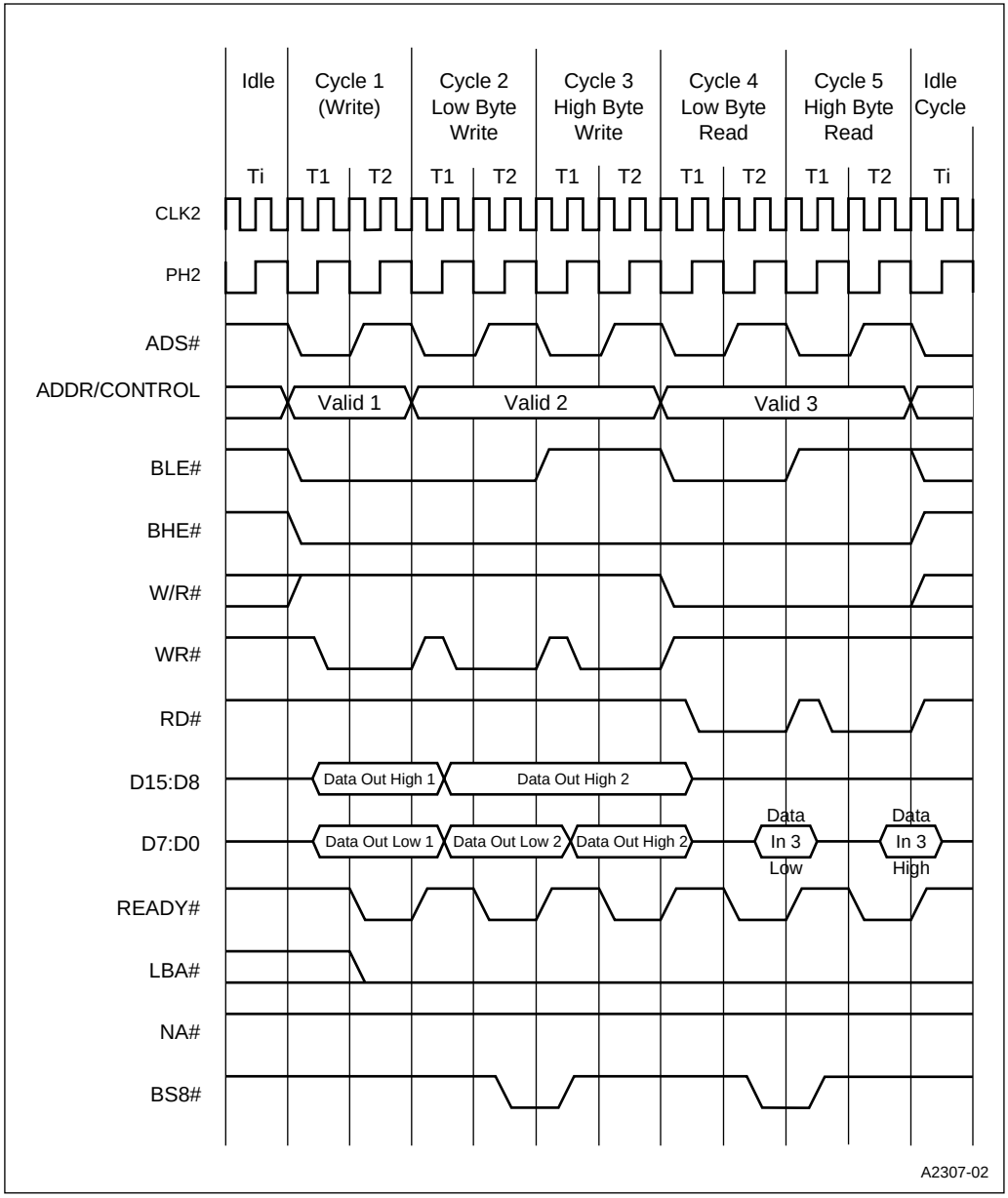

Figure 19. Local Bus Read and Write BS8# Cycles

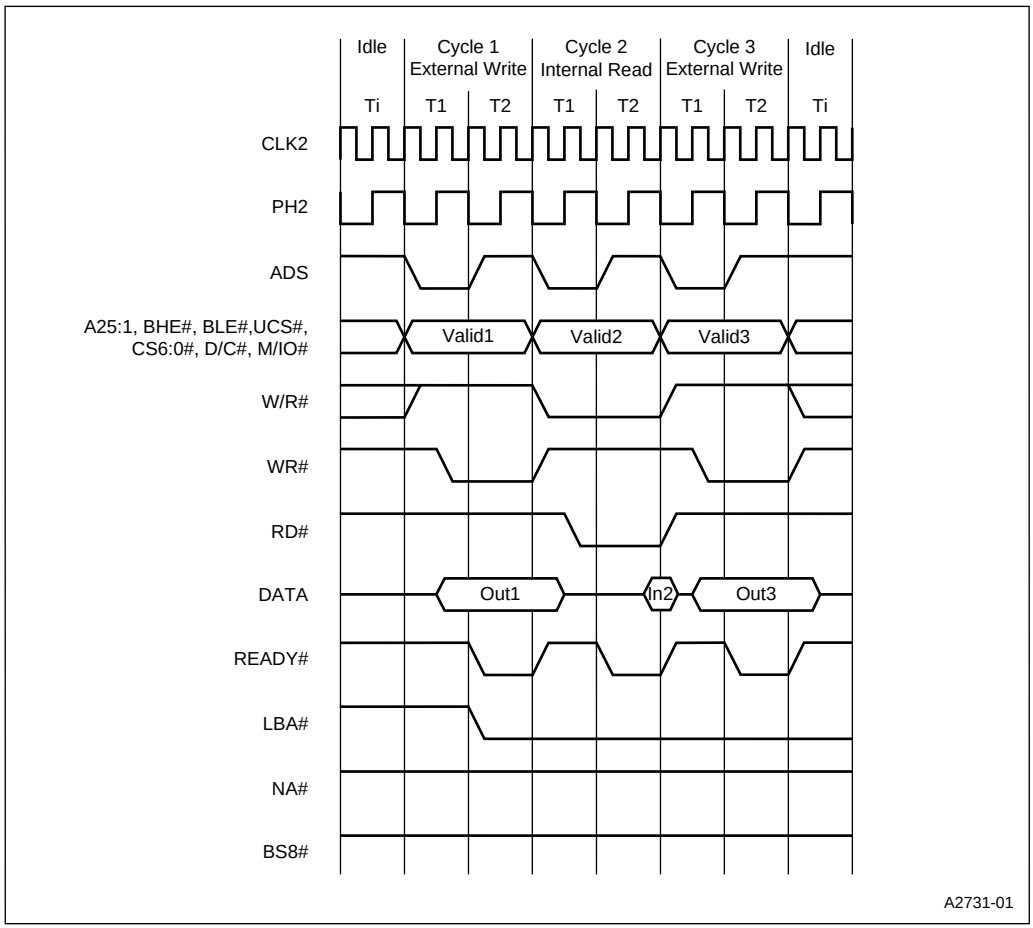

Figure 20. Local Bus Read and Write Cycles (Internal and External)

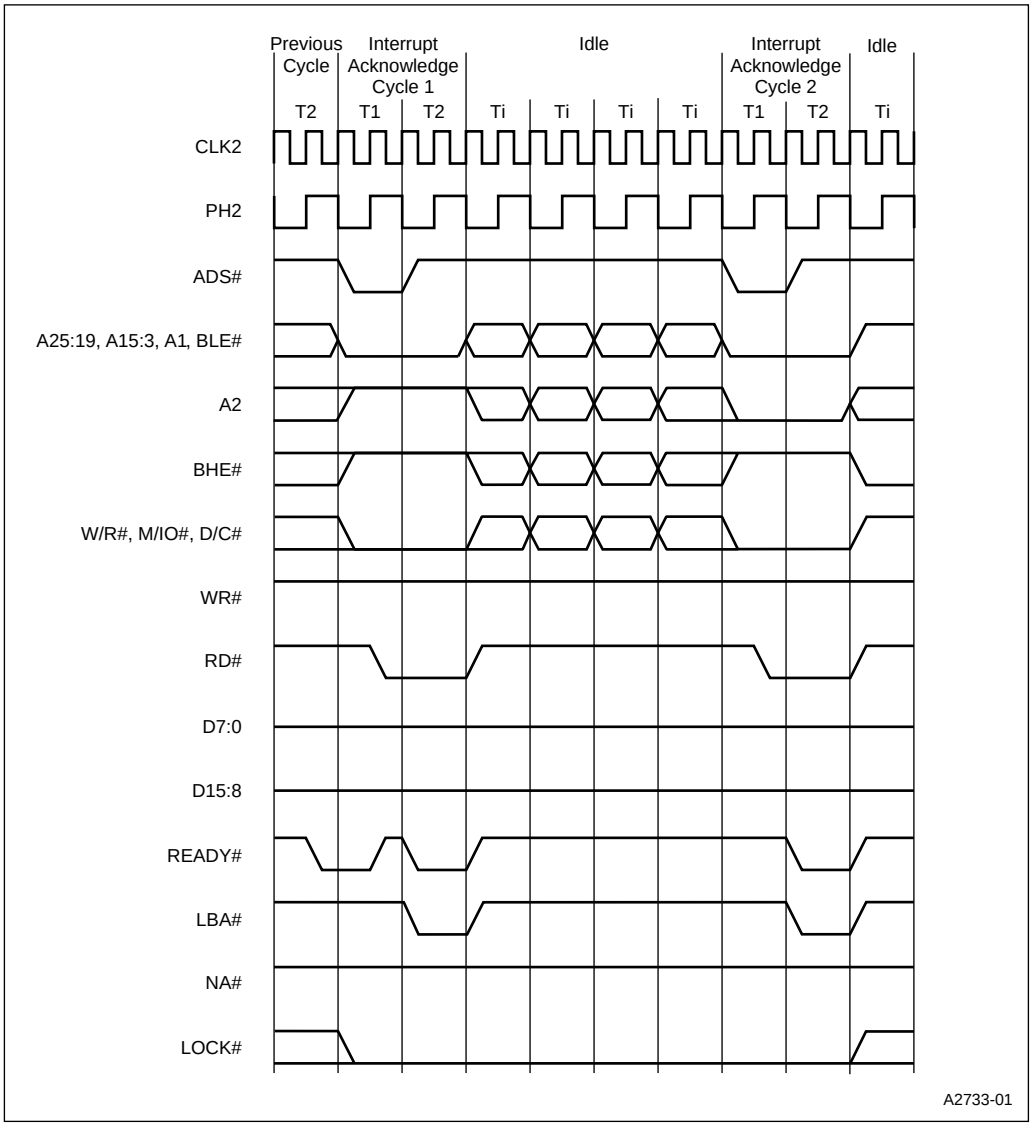

Figure 21. Local Bus Interrupt Acknowledge Cycle (Internal Cascade)

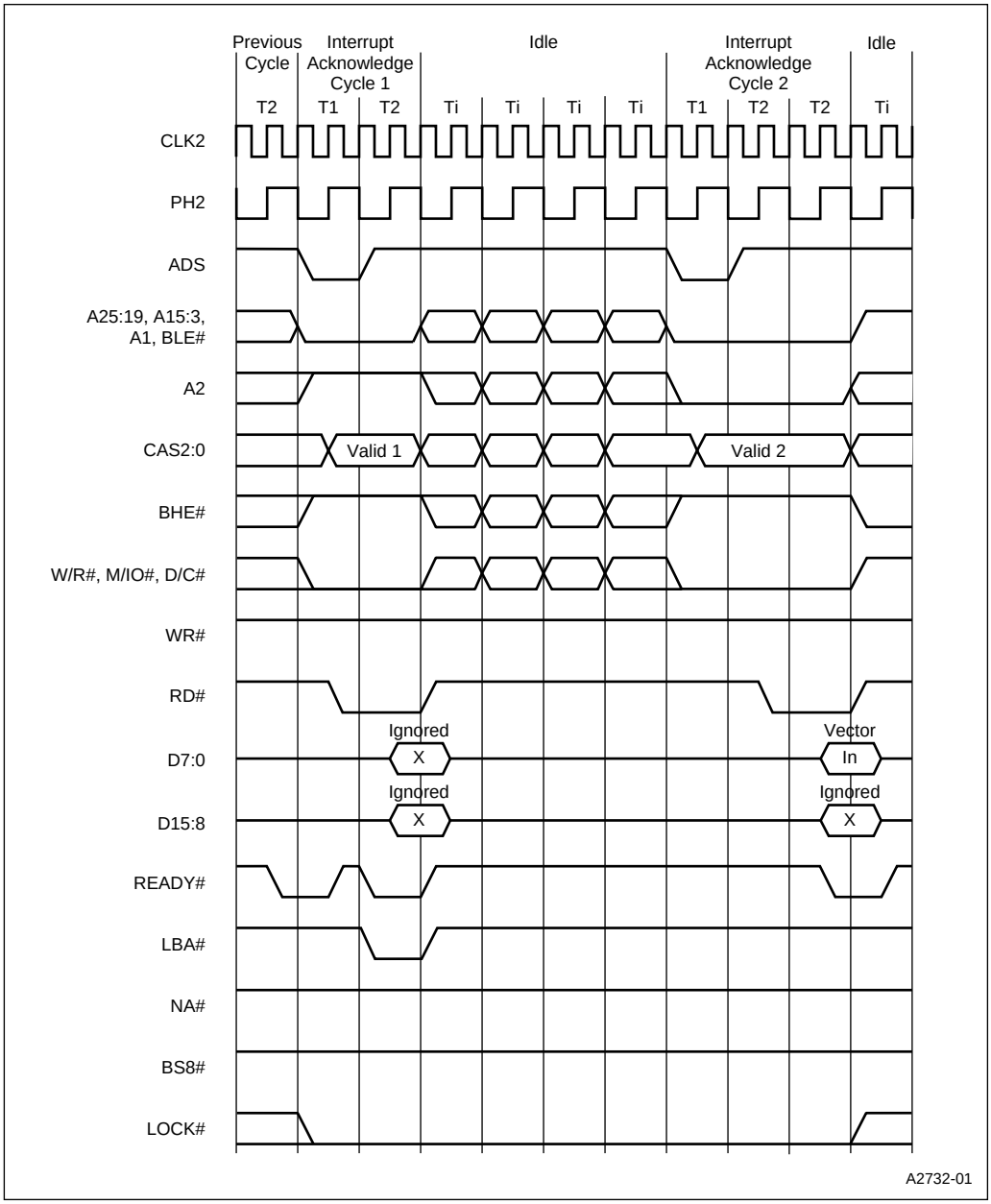

Figure 22. Local Bus Interrupt Acknowledge Cycle (External Cascade)

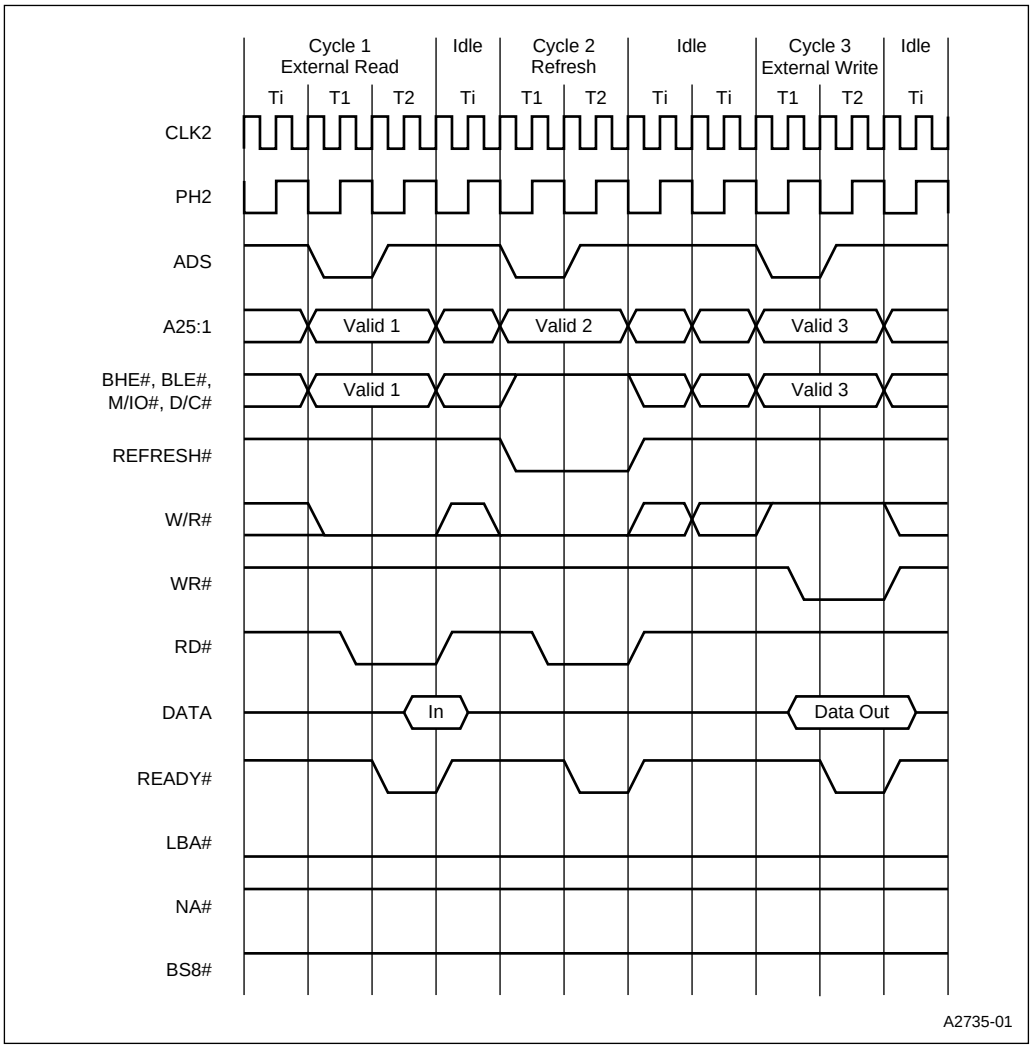

Figure 23. Local Bus Nonpipelined Refresh Cycle

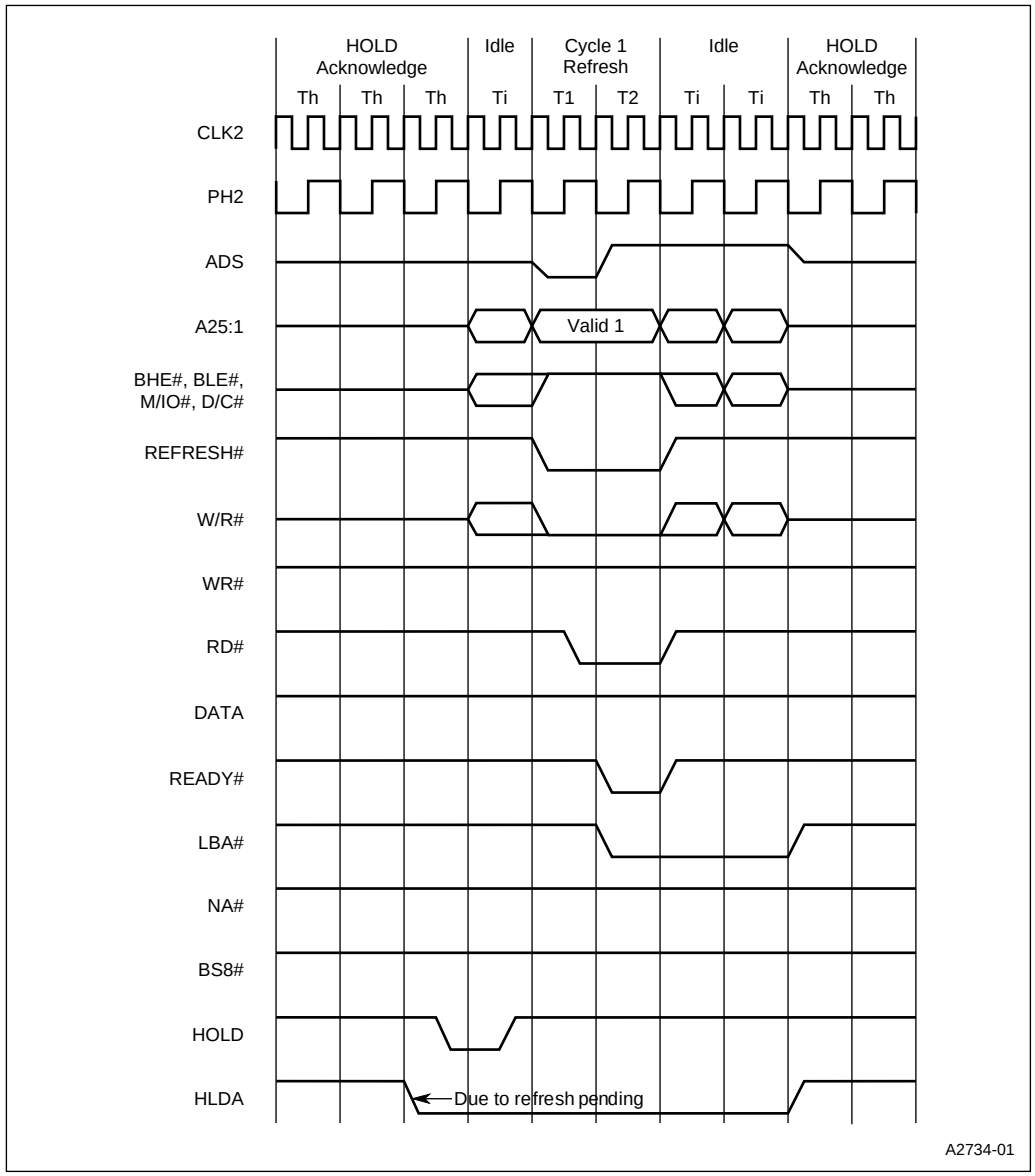

Figure 24. Local Bus Refresh Cycle During HOLD/HLDA

8.0 REVISION HISTORY

This data sheet (272420-004) is valid for devices marked with a “B” at the end of the top side tracking number. Data sheets are changed as new device information becomes available. Verify with your local Intel sales office that you have the latest version before finalizing a design or ordering devices.

This -004 data sheet contains the following changes from the -003 version.

- The -003 data sheet was valid for devices marked with an “A” at the end of the top side tracking number
- A significant number of pinout assignments have changed in the 144 pin TQFP package (Figure 3 and Table 2)
- Section 4.3 “Package Thermal Characteristics” has been added
- The separate V_{IL1} and V_{IL1} specs were removed
- Some corrections were added to the text describing RD#, WR#, READY# (out), and BS8# phase relationships in section 6.0
- Correction made to BS8# input in the “Drive Levels and Measurement Points for AC Specifications” figure. Also, drive levels for inputs were changed to V_{CC} and V_{SS} in this figure
- The following AC Timings were updated in Table 7:
  t6, t8a, t12, t14, t15, t34, t43, t44, t45, t46, t47, t48, t52, t115, t116, t127, t128
- The following new AC Timings were added to Table 7:
  t10a, t19a, t41a, t42a, t47a, t51a, t112, t113, t114, t118, t119, t120, t121, t122, t123, t124, t125, t126
- The following AC Timing Waveforms were updated:
  Input Setup and Hold Timing
  Output Valid Delay Timing
  Output Float Delay and HLDA Valid Delay Timing
- The following new AC Timing Waveforms were added:
  Relative Signal Timing
  SSIO Timing
  Timer/Counter Timing
- Section 7 - Bus Cycle Waveforms has been added
- This revision history has been added