NOTE: The Intel Architecture Software Developer’s Manual consists of the following volumes: Basic Architecture, Order Number 243190; Instruction Set Reference, Order Number 243191; Addendum to the Instruction Set Reference, Order Number 243689; System Programming Guide, Order Number 243192; and the Addendum to the System Programming Guide, Order Number 243690. Please refer to all of these volumes when evaluating your design needs.
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>CHAPTER 10</th>
<th>PROCESSOR IDENTIFICATION AND FEATURE DETERMINATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.1.</td>
<td>CPUID INSTRUCTION EXTENSIONS</td>
</tr>
<tr>
<td>10.1.1.</td>
<td>Version Information</td>
</tr>
<tr>
<td>10.1.2.</td>
<td>Control Register Extensions</td>
</tr>
</tbody>
</table>
When writing software intended to run on several different types of Intel Architecture processors, it is generally necessary to identify the type of processor present in a system and the processor features that are available to an application. This chapter describes how to identify the processor that is executing the code and determine the features the processor supports. It also shows how to determine if an FPU or NPX is present. For more information about processor identification and supported features, refer to the following documents:

- AP-485, *Intel Processor Identification and the CPUID Instruction*
- For a complete list of the features that are available for the different Intel Architecture processors, refer to Chapter 17 of the *Intel Architecture Software Developer’s Manual, Volume 3: System Programming Guide.*

### 10.1. CPUID INSTRUCTION EXTENSIONS

The CPUID instruction of all P6 family processors behave identically. The CPUID instruction is described in detail in the application note, AP-485, *Intel Processor Identification and the CPUID Instruction.* This section describes processor-specific information returned by the CPUID instruction.

The CPUID instruction's behavior varies depending upon the contents of the EAX register when the instruction is executed. Table 10-1 shows the interaction between the value in EAX before the call to CPUID and the value that CPUID returns.
Table 10-1. EAX Input Value and CPUID Return Values

<table>
<thead>
<tr>
<th>EAX</th>
<th>CPUID Return Values</th>
</tr>
</thead>
</table>
| 0   | EAX Maximum CPUID input value  
|     | EBX 756E6547H 'uneG' (G in BL)  
|     | EDX 49656E69H 'ieni' (i in DL)  
|     | ECX 6C65746EH 'letn' (n in CL)  |
| 1   | EAX Version information (Type, Family, Model, Stepping)  
|     | EBX Reserved  
|     | EDX Reserved  
|     | ECX Feature information  |
| 2   | EAX Cache Information  
|     | EBX Cache Information  
|     | EDX Cache Information  
|     | ECX Cache Information  |

Refer to the CPUID application note, AP-485, for details on cache information. AP-485 is available from the following web site: http://developer.intel.com/design/pro/applnots/ap485.htm.

In addition, the following two new cache descriptors are defined for P6 family processors with Model > 3:

- 1M L2 Cache  
  4-way set associative  
  32-byte line size  
  44h
- 2M L2 Cache  
  4-way set associative  
  32-byte line size  
  45h

10.1.1. Version Information

When the CPUID instruction is executed with a 1 in EAX, it returns version and feature information. Figure 10-1 shows the version information bit fields returned by CPUID in EAX. The 233, 266, and 300 MHz Pentium® II processors are indicated by a ‘6’ in the Family ID and a ‘3’ in the Model ID field. Future P6 family processors are indicated by a ‘6’ in the Family ID and a value greater than ‘3’ in the Model ID field.
PROCESSOR IDENTIFICATION AND FEATURE DETERMINATION

![Figure 10-1. Processor Version Information Returned by CPUID in EAX](image)

Figure 10-1 shows the feature information bit fields returned by CPUID in EDX.

![Figure 10-2. Feature Information Returned by CPUID in EDX](image)

Figure 10-2 shows the feature information bit fields returned by CPUID in EDX.

Table 10-2 describes the bit representations for the new P6 family processor features.

### Table 10-2. New P6 Family Processor Feature Information Returned by CPUID in EDX

<table>
<thead>
<tr>
<th>Bit</th>
<th>Feature</th>
<th>Value</th>
<th>Description</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>11</td>
<td>SEP</td>
<td>1</td>
<td>Fast System Call</td>
<td>Indicates whether the processor supports the Fast System Call instructions, SYSENTER and SYSEXIT.</td>
</tr>
<tr>
<td>23</td>
<td>MMX</td>
<td>1</td>
<td>MMX-technology</td>
<td>Indicates whether the processor supports the MMX-technology instruction set and architecture.</td>
</tr>
</tbody>
</table>

Table 10-3 describes the bit representations for new P6 family processor features.
PROCESSOR IDENTIFICATION AND FEATURE DETERMINATION

Table 10-3. New P6 Family Processor Feature Information Returned by CPUID in EDX

<table>
<thead>
<tr>
<th>Bit</th>
<th>Feature</th>
<th>Value</th>
<th>Description</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>PAT</td>
<td>1</td>
<td>Page Attribute Table</td>
<td>Indicates whether the processor supports the Page Attribute Table. This feature augments the Memory Type Range Registers (MTRRs), allowing an operating system to specify attributes of memory on a page granularity through a linear address.</td>
</tr>
<tr>
<td>17</td>
<td>PSE-36</td>
<td>1</td>
<td>36-bit Page Size Extension</td>
<td>Indicates whether the processor supports 4 MB pages that are capable of addressing physical memory beyond 4 GB. This feature indicates that the upper four bits of the physical address of the 4-MB page is encoded by bits 13-16 of the page directory entry.</td>
</tr>
<tr>
<td>18-22</td>
<td>rsvd</td>
<td>0</td>
<td>Reserved</td>
<td>These bits are reserved for future use. The contents of these fields are not defined and should not be relied upon or altered.</td>
</tr>
<tr>
<td>24</td>
<td>FXSR</td>
<td>1</td>
<td>Fast floating point save and restore</td>
<td>Indicates whether the processor supports the FXSAVE and FXRSTOR instructions for fast save and restore of the floating point context. Presence of this bit also indicates that CR4.OSFXSR is available, allowing an operating system to indicate that it uses the fast save/restore instructions.</td>
</tr>
</tbody>
</table>

10.1.2. Control Register Extensions

The control registers (CR0, CR1, CR2, CR3 and CR4) determine the operating mode of the processor and the characteristics of the currently executing task. A new field has been added to CR4, which contains a group of flags used to enable several architectural extensions as depicted in Figure 10-3.

<table>
<thead>
<tr>
<th>31</th>
<th>10</th>
<th>09</th>
<th>08</th>
<th>07</th>
<th>06</th>
<th>05</th>
<th>04</th>
<th>03</th>
<th>02</th>
<th>01</th>
<th>00</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Reserved (set to 0)</td>
<td>OSFXSR</td>
<td>PCE</td>
<td>PGE</td>
<td>MCE</td>
<td>PAE</td>
<td>PSE</td>
<td>DE</td>
<td>TSD</td>
<td>PVI</td>
<td>VME</td>
</tr>
</tbody>
</table>

Figure 10-3. CR4 Register Extensions

The new field at bit 9 (OSFXSR) is set by the operating system to indicate that it uses the FXSAVE/FXRSTOR instructions for saving/restoring FP/MMX state during context switches. This bit defaults to clear (zero) at processor initialization.
UNITED STATES, Intel Corporation
2200 Mission College Blvd., P.O. Box 58119, Santa Clara, CA  95052-8119
Tel: +1 408 765-8080

JAPAN, Intel Japan K.K.
5-6 Tokodai, Tsukuba-shi, Ibaraki-ken  300-26
Tel: + 81-29847-8522

FRANCE, Intel Corporation S.A.R.L.
1, Quai de Grenelle, 75015  Paris
Tel: +33 1-45717171

UNITED KINGDOM, Intel Corporation (U.K.) Ltd.
Pipers Way, Swindon, Wiltshire, England SN3 1RJ
Tel: +44 1-793-641440

GERMANY, Intel GmbH
Dornacher Strasse 1
85622 Feldkirchen/ Muenchen
Tel: +49 89/99143-0

HONG KONG, Intel Semiconductor Ltd.
32/F Two Pacific Place, 88 Queensway, Central
Tel: +852 2844-4555

CANADA, Intel Semiconductor of Canada, Ltd.
190 Attwell Drive, Suite 500
Rexdale, Ontario  M9W 6H8
Tel: +416 675-2438